

Compal Confidential

PEW72/82/92 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRIII + ICH9M

2010-07-09

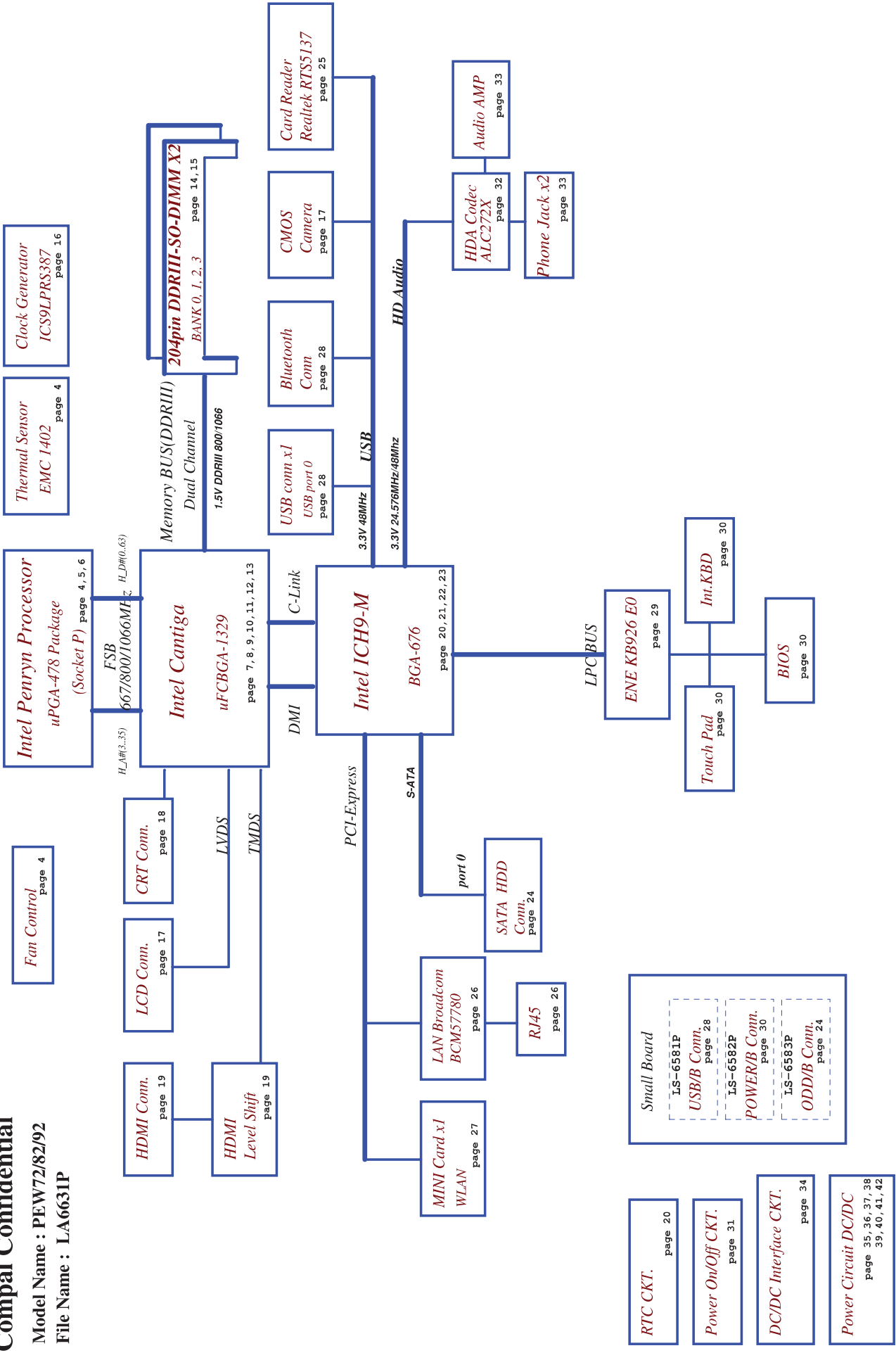
REV:1.0

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Issued Date		2010/04/22	Deciphered Date	2011/04/22	
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		Document Number		PEW72/82 M/B LA-6631P Schematic	
		Revision		1.0	
		Date		Fri Jul 09 2010	
		Sheet		1 of 44	

Compal Confidential

Model Name : PEW72/82/92

File Name : LA6631P



Security Classification		Compal Secret Data		Title	
Issued Date	2010/04/22	Deciphered Date	2011/04/22	Block Diagrams	
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Document Number				PEW72/82 M/B LA-6631P Schematic	
Date				130602	

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V power rail for DDR	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for LVDS	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5VB	5V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	SMSC EMC1402	100 1100 b

EC SM Bus2 address

ICH9M SM Bus address

Device	Address
Clock Generator (IC9SLVRS87, RTMB90N)	1101 001Xb
DDR DIMM1	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%		
Ra/Rc/Re	100K +/- 5%		
Board ID	Rb / Rd / Rf	VAD_BID_min	VAD_BID_max
0	0	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.289 V
2	18K +/- 5%	0.436 V	0.538 V
3	33K +/- 5%	0.712 V	0.875 V
4	56K +/- 5%	1.036 V	1.264 V
5	100K +/- 5%	1.453 V	1.759 V
6	200K +/- 5%	1.935 V	2.341 V
7	NC	2.500 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
GM45 B3	GM@
GM45 A1	GMAL@
GL40 B3	GL@
GM40 A1	GLA1@
Bluetooth	BT@

PCIE table

PCIE port1	
PCIE port2	Wireless Card
PCIE port3	PCIE LAN
PCIE port4	
PCIE port5	
PCIE port6	

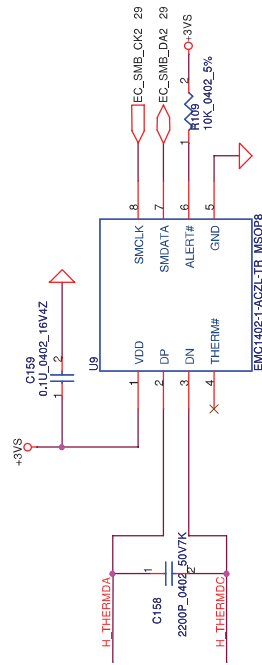
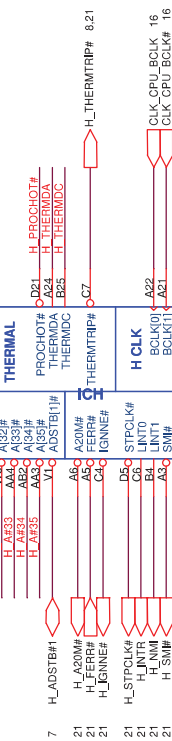
USB table

EHC11	UHC11	Port0	MB USB Conn.
		Port1	USB/B Conn.
	UHC12	Port2	
		Port3	CMOS Camera
	UHC13	Port4	Card Reader
EHC12		Port5	
	UHC14	Port6	USB/B Conn.
		Port7	
	UHC15	Port8	Blue Tooth
		Port9	
	UHC16	Port10	Wireless Card
		Port11	


SATA table

SATA port0	HDD
SATA port1	ODD
SATA port2	
SATA port3	
SATA port4	
SATA port5	

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Date				10/26/2010



PCB

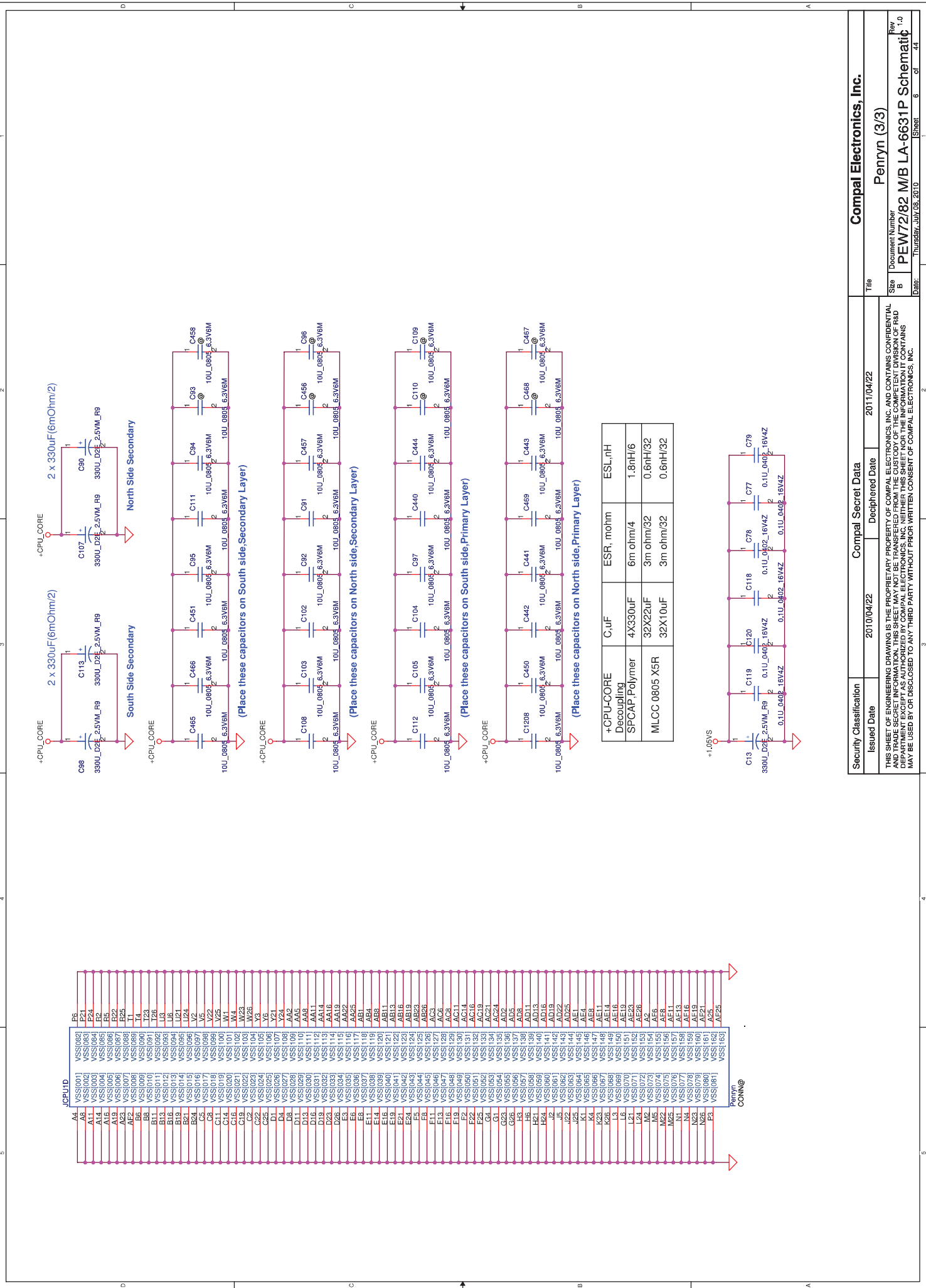


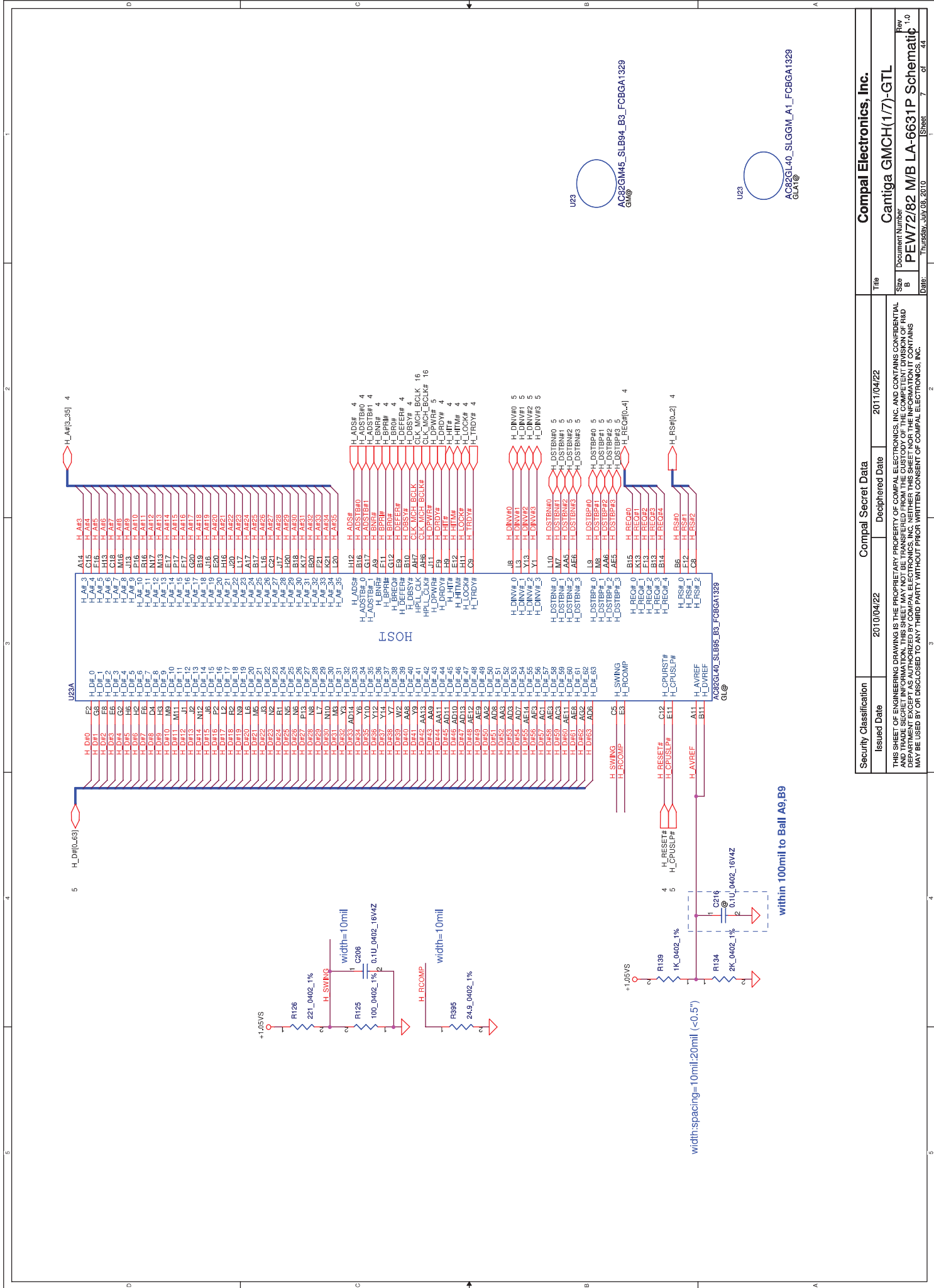
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LA-6631P MB Rev.1: DAZ00000IU10
LA-6631P MB with Small Board Ver.: DAZ0FZ00100

LA-6631P MB Rev.1
DAZ0FZ00100
PCB FEW72 LA-6631P LS-6581P/6582P/6583P

LA-6631P MB Rev1: DA60000IU10
LA-6631P MB with Small Board Rev1: DAZ0FZ00100

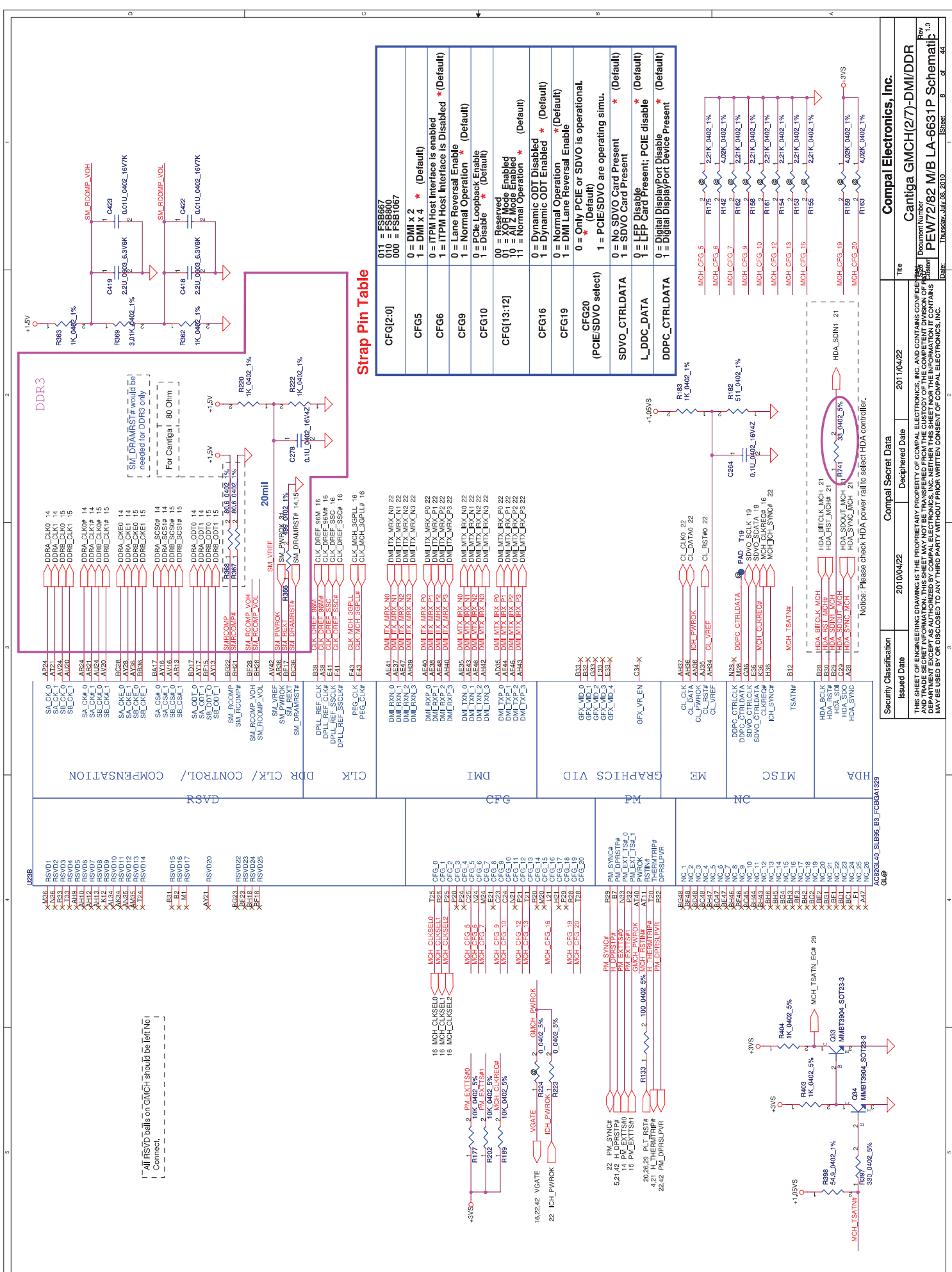
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				Penryn (1/3) & FAN	
Size	Document Number			Rev	
B	PEW2782			1.0	
Date:	Thursday, Jul 08, 2010			Issue	





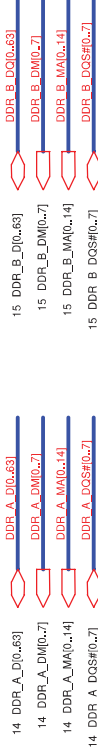
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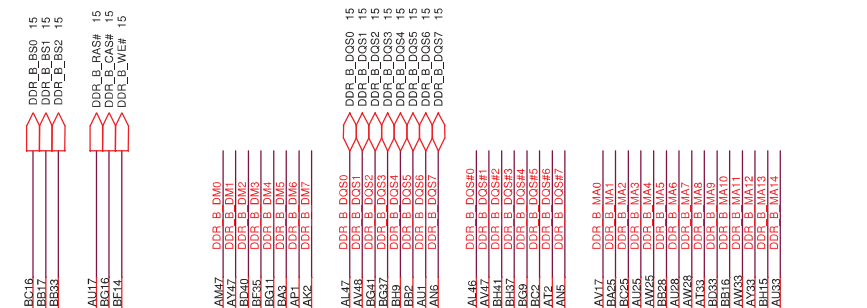
Strap Pin Table

CFG2[0]	011 = FSB967 010 = FSB960 000 = FSB1067
CFG5	0 = DMI x 2 * (Default)
CFG6	0 = ITPM Host Interface is Disabled * (Default) 1 = ITPM Host Interface is Enabled
CFG9	0 = Lane Reversal Enable * (Default) 1 = Normal Operation
CFG10	0 = PCIe Loopback Enable * (Default) 1 = Disable
CFG13[12]	00 = Reserved 01 = XOP Mode Enabled 10 = XOP Mode Disabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled * (Default) 1 = Dynamic ODT Enabled
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
CFG20	0 = Only PCIe or SDVO is operational. 1 = PCIe/SDVO are operating simul.
SDVO_CTRLDATA	0 = No SDVO Card Present * (Default) 1 = SDVO Card Present
L_DDC_DATA	0 = Display Present; PCIe disable * (Default) 1 = LFP Card Present
DDPC_CTRLDATA	0 = Digital DisplayPort Disable * (Default) 1 = Digital DisplayPort Device Present



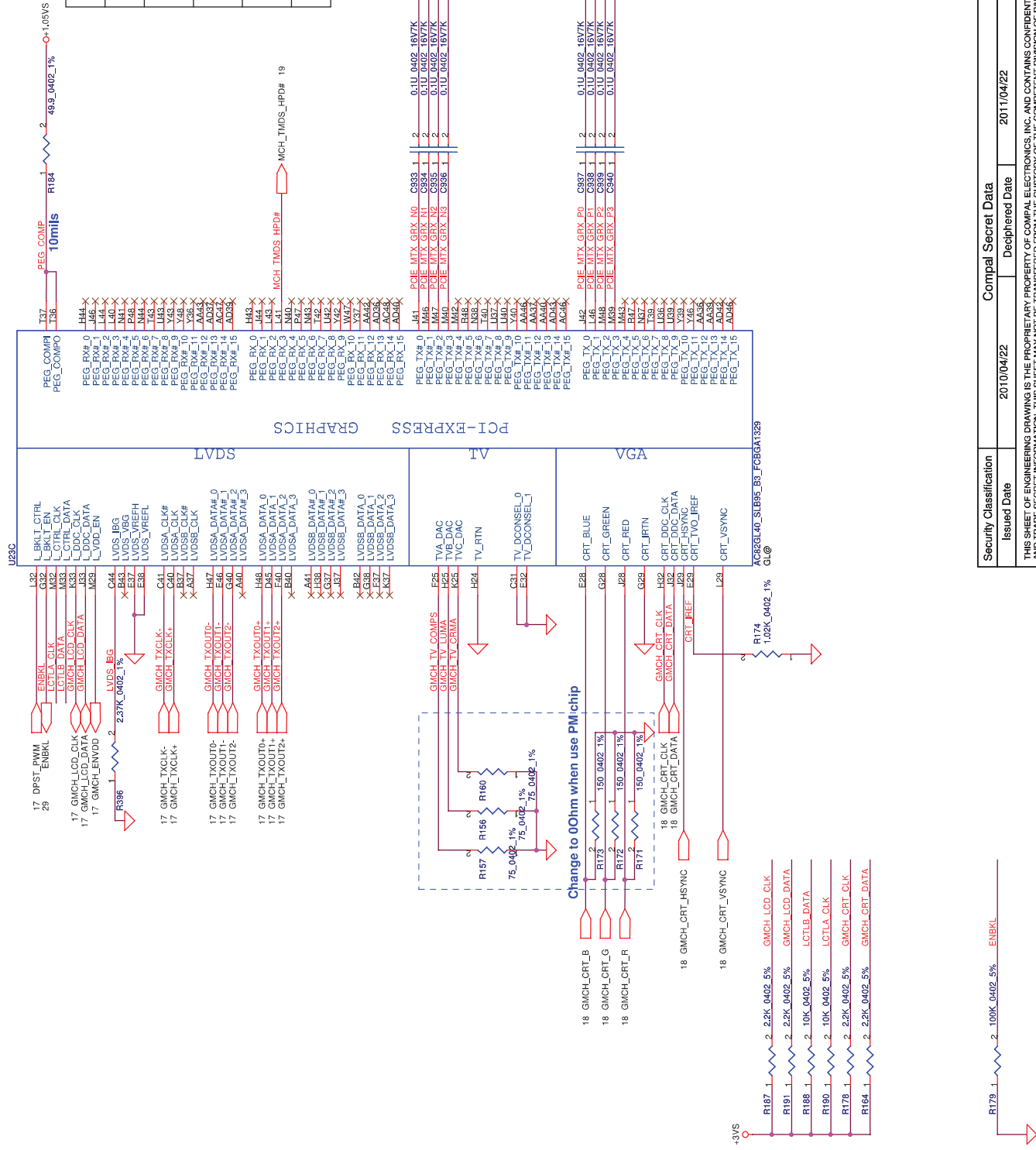
U23D		
DDR_A_D0	A138	SA_BS_0
DDR_A_D1	A141	SA_BS_1
DDR_A_D2	A138	SA_BS_2
DDR_A_D3	A139	SA_BS_3
DDR_A_D4	A138	SA_BS_4
DDR_A_D5	A140	SA_BS_5
DDR_A_D6	A144	SA_BS_6
DDR_A_D7	A142	SA_BS_7
DDR_A_D8	A143	SA_BS_8
DDR_A_D9	A144	SA_BS_9
DDR_A_D10	A138	SA_BS_10
DDR_A_D11	A141	SA_BS_11
DDR_A_D12	A142	SA_BS_12
DDR_A_D13	A143	SA_BS_13
DDR_A_D14	A144	SA_BS_14
DDR_A_D15	A142	SA_BS_15
DDR_A_D16	A139	SA_BS_16
DDR_A_D17	A140	SA_BS_17
DDR_A_D18	A141	SA_BS_18
DDR_A_D19	B143	SA_BS_19
DDR_A_D20	A141	SA_BS_20
DDR_A_D21	A143	SA_BS_21
DDR_A_D22	B140	SA_BS_22
DDR_A_D23	B140	SA_BS_23
DDR_A_D24	A143	SA_BS_24
DDR_A_D25	B138	SA_BS_25
DDR_A_D26	A137	SA_BS_26
DDR_A_D27	A138	SA_BS_27
DDR_A_D28	B138	SA_BS_28
DDR_A_D29	B138	SA_BS_29
DDR_A_D30	A138	SA_BS_30
DDR_A_D31	A138	SA_BS_31
DDR_A_D32	A138	SA_BS_32
DDR_A_D33	A111	SA_BS_33
DDR_A_D34	B112	SA_BS_34
DDR_A_D35	B112	SA_BS_35
DDR_A_D36	A137	SA_BS_36
DDR_A_D37	A137	SA_BS_37
DDR_A_D38	B112	SA_BS_38
DDR_A_D39	B112	SA_BS_39
DDR_A_D40	B112	SA_BS_40
DDR_A_D41	A110	SA_BS_41
DDR_A_D42	A110	SA_BS_42
DDR_A_D43	A110	SA_BS_43
DDR_A_D44	B111	SA_BS_44
DDR_A_D45	B111	SA_BS_45
DDR_A_D46	B111	SA_BS_46
DDR_A_D47	B111	SA_BS_47
DDR_A_D48	A110	SA_BS_48
DDR_A_D49	A110	SA_BS_49
DDR_A_D50	A110	SA_BS_50
DDR_A_D51	A110	SA_BS_51
DDR_A_D52	A110	SA_BS_52
DDR_A_D53	A110	SA_BS_53
DDR_A_D54	A110	SA_BS_54
DDR_A_D55	A110	SA_BS_55
DDR_A_D56	A110	SA_BS_56
DDR_A_D57	A110	SA_BS_57
DDR_A_D58	A110	SA_BS_58
DDR_A_D59	A110	SA_BS_59
DDR_A_D60	A110	SA_BS_60
DDR_A_D61	A110	SA_BS_61
DDR_A_D62	A110	SA_BS_62
DDR_A_D63	A110	SA_BS_63

U23E		
DDR_B_D0	A147	SB_BS_0
DDR_B_D1	A146	SB_BS_1
DDR_B_D2	A147	SB_BS_2
DDR_B_D3	A146	SB_BS_3
DDR_B_D4	A146	SB_BS_4
DDR_B_D5	A148	SB_BS_5
DDR_B_D6	A148	SB_BS_6
DDR_B_D7	A148	SB_BS_7
DDR_B_D8	A148	SB_BS_8
DDR_B_D9	A146	SB_BS_9
DDR_B_D10	B148	SB_BS_10
DDR_B_D11	A148	SB_BS_11
DDR_B_D12	A147	SB_BS_12
DDR_B_D13	A147	SB_BS_13
DDR_B_D14	B147	SB_BS_14
DDR_B_D15	B147	SB_BS_15
DDR_B_D16	B146	SB_BS_16
DDR_B_D17	B146	SB_BS_17
DDR_B_D18	B146	SB_BS_18
DDR_B_D19	B146	SB_BS_19
DDR_B_D20	B146	SB_BS_20
DDR_B_D21	B146	SB_BS_21
DDR_B_D22	B146	SB_BS_22
DDR_B_D23	B146	SB_BS_23
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DDR_B_D25	B146	SB_BS_25
DDR_B_D26	B146	SB_BS_26
DDR_B_D27	B146	SB_BS_27
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DDR_B_D38	B146	SB_BS_38
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DDR_B_D49	B146	SB_BS_49
DDR_B_D50	B146	SB_BS_50
DDR_B_D51	B146	SB_BS_51
DDR_B_D52	B146	SB_BS_52
DDR_B_D53	B146	SB_BS_53
DDR_B_D54	B146	SB_BS_54
DDR_B_D55	B146	SB_BS_55
DDR_B_D56	B146	SB_BS_56
DDR_B_D57	B146	SB_BS_57
DDR_B_D58	B146	SB_BS_58
DDR_B_D59	B146	SB_BS_59
DDR_B_D60	B146	SB_BS_60
DDR_B_D61	B146	SB_BS_61
DDR_B_D62	B146	SB_BS_62
DDR_B_D63	B146	SB_BS_63

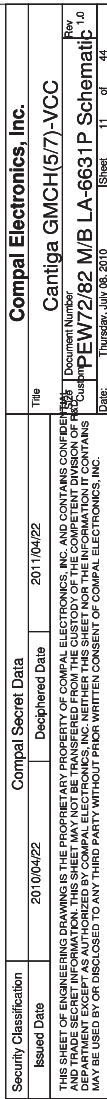


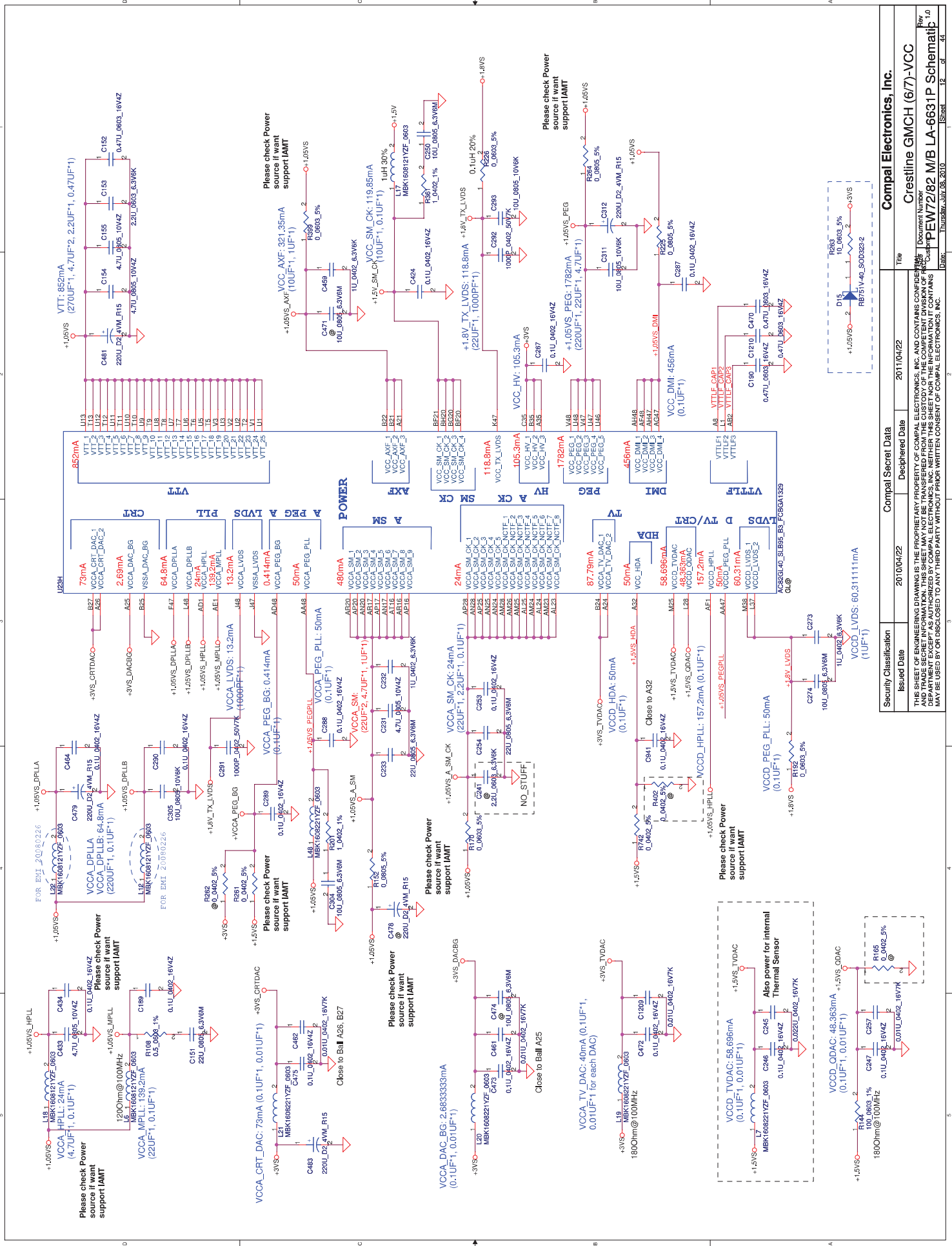
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Compal Electronics, Inc.

Crestline GMCH (6/7)-VCC

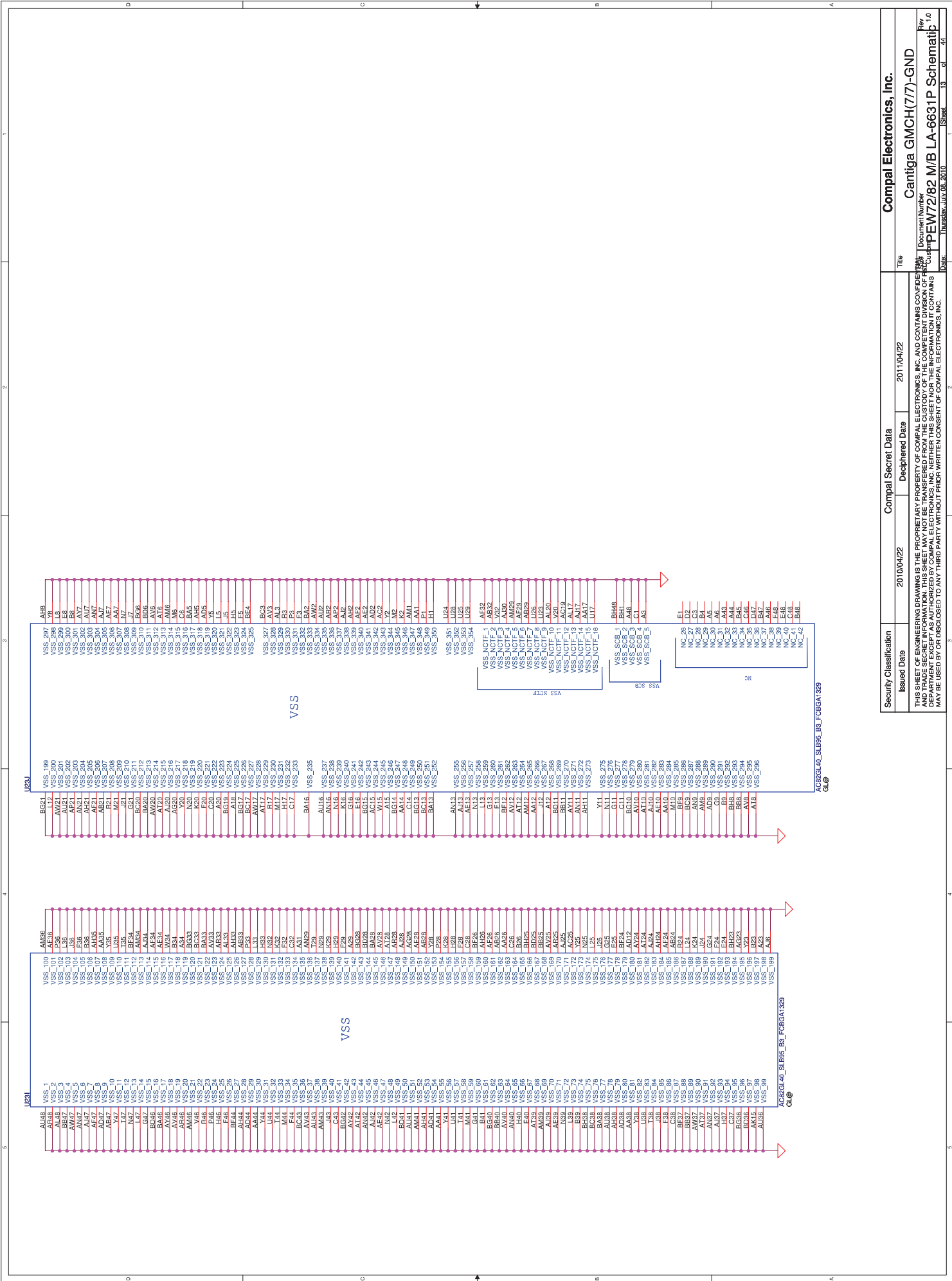
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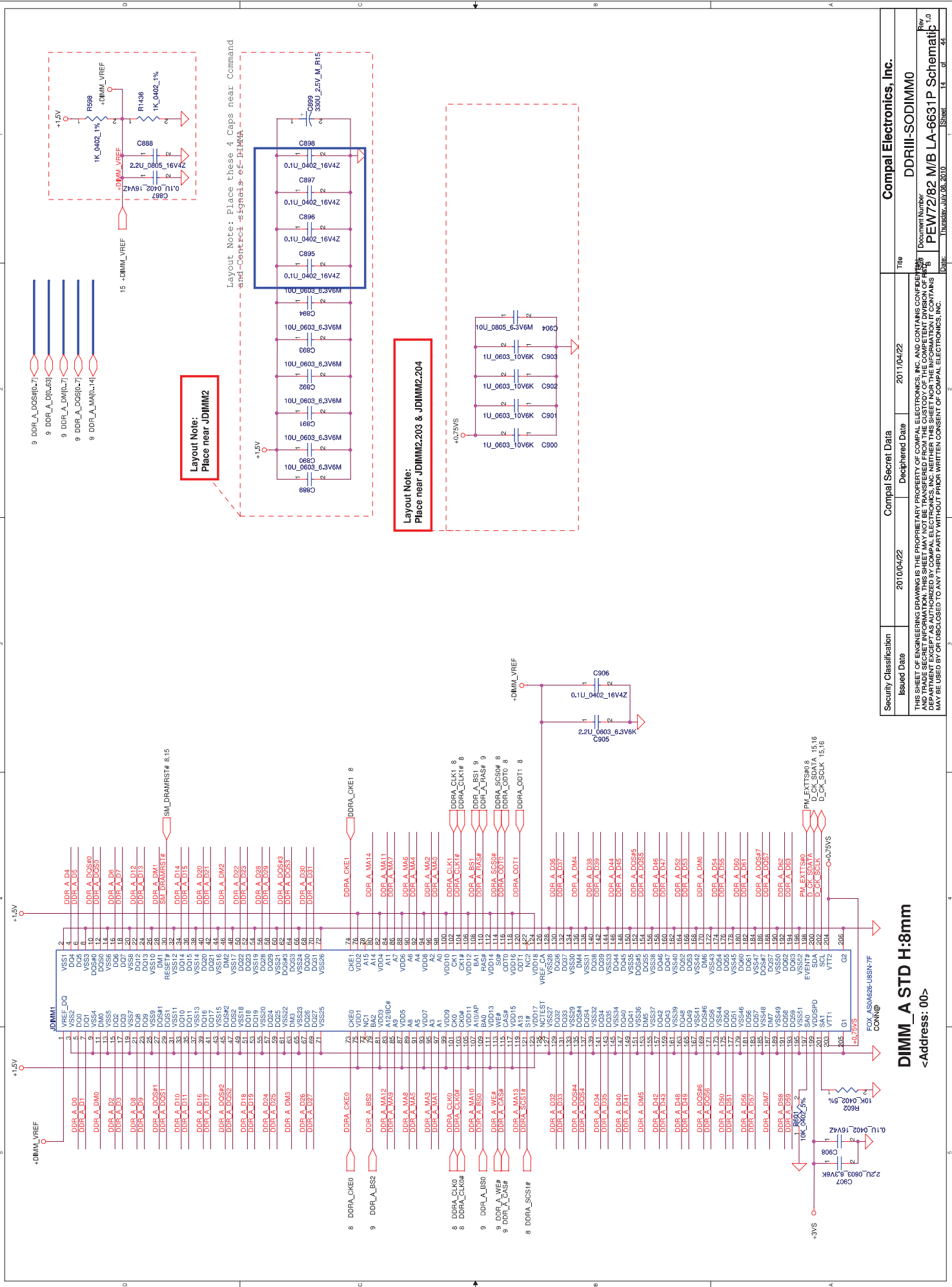
PEW7282 M/B LA-6631P Schematic

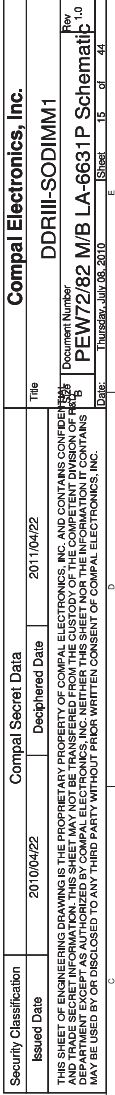
Rev 1.0

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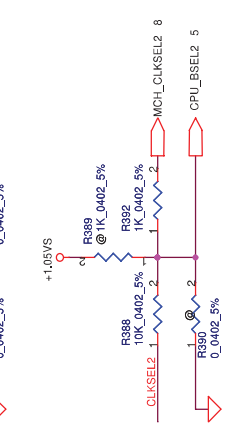
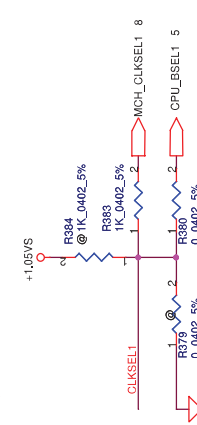
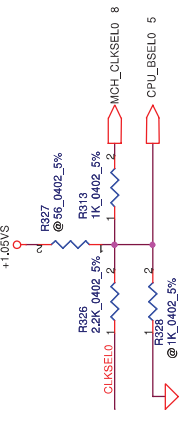
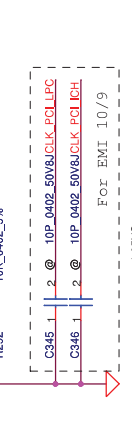
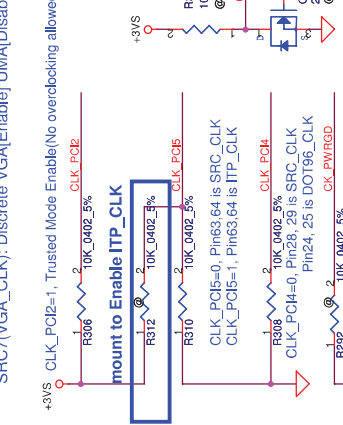
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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	0	1	200	100	33.3
0	1	1	166	100	33.3

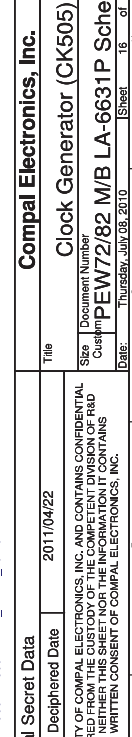
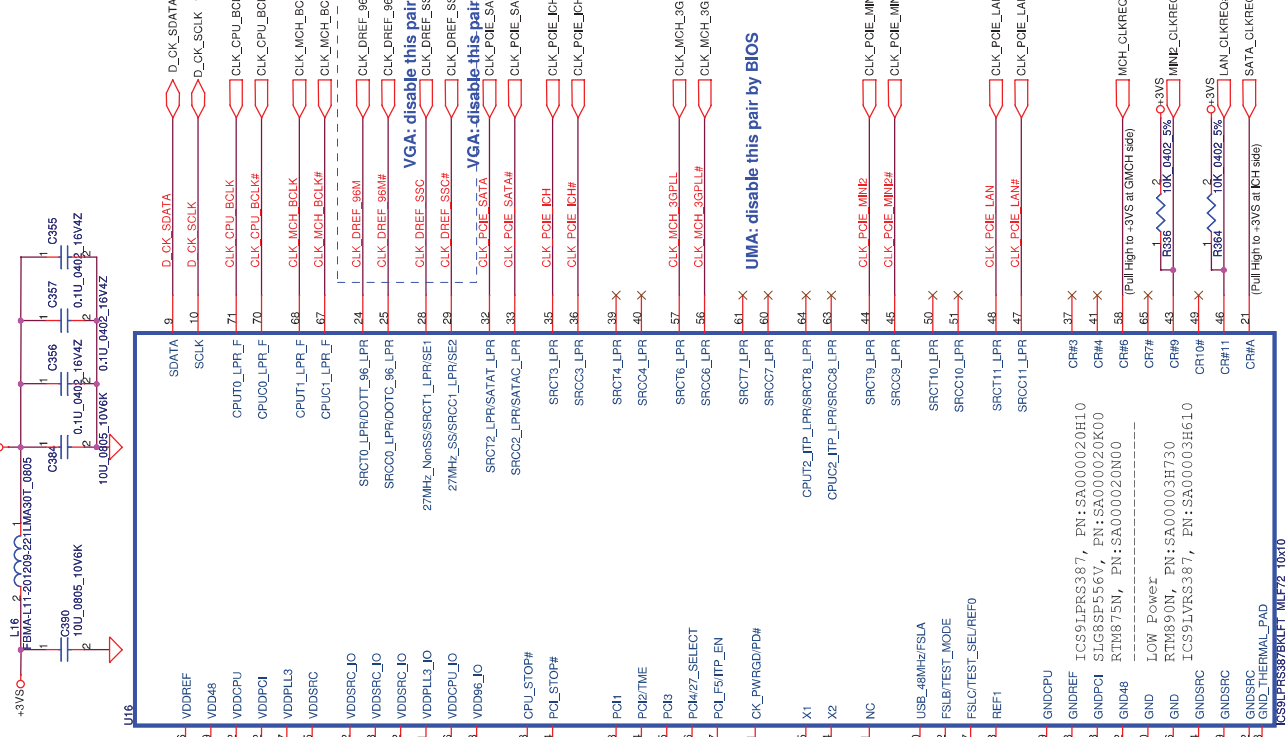
Table : ICS9LPRS387

CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PCIEX0
CR#_6(MCH)	PCIEX6	PCIEX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

SPC3/VCA CLK. Please VCA Enable! 11/14/2016



Clock Generator



Compal Electronics, Inc.

Number	Sheet	of
172/82 M/B LA-6631P Schee	16	
Day, July 08, 2010		

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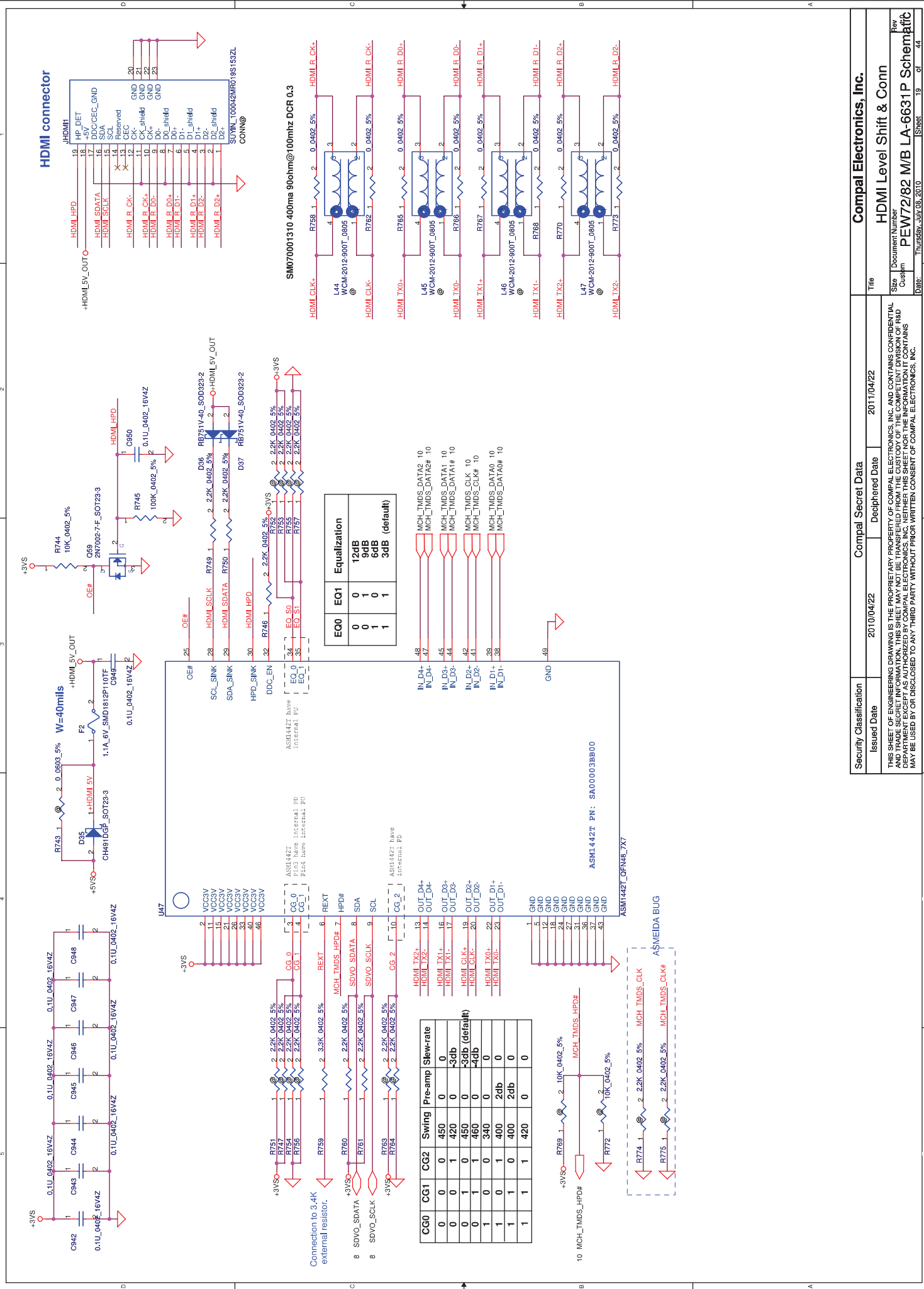
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6		

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6		

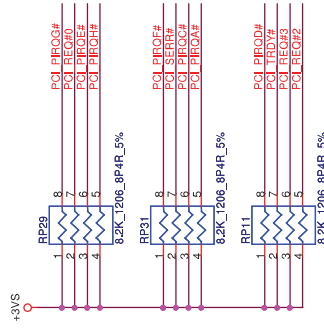
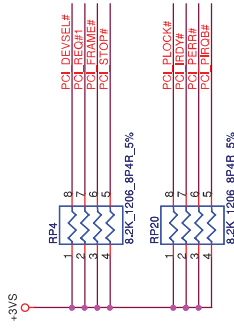
5		
6		

Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.
Issued Date	2010/04/22	Declassified Date		CRT Connector
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			Document Number	PEW72/82 M/B LA-6631P Schematic 1.0
			Date	Thursday, July 08, 2010
			Sheet	18 of 44

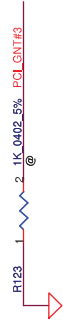


Security Classification		Compal Secret Data		Title	
Issued Date	2010/04/22	Deciphered Date	2011/04/22	HDMI Level Shift & Conn	
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Size		Document Number		Rev	
Custpm		PEW72/82 M/B LA-6631P Schematic			
Date:		Thursday, July 08, 2010		Sheet 19 of 44	

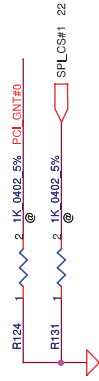
Security Classification		Compal Secret Data		Title	
Issued Date	2010/04/22	Deciphered Date	2011/04/22	HDMI Level Shift & Conn	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					
Size		Document Number		Rev	
Custpm		PEW72/82 M/B LA-6631P Schematic			
Date		Thursday, July 08, 2010		Sheet 19 of 44	



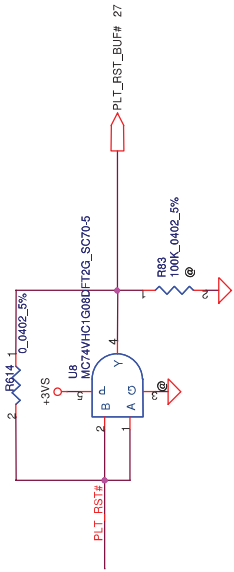
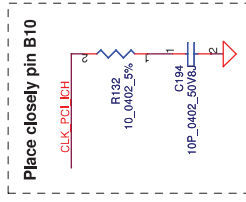
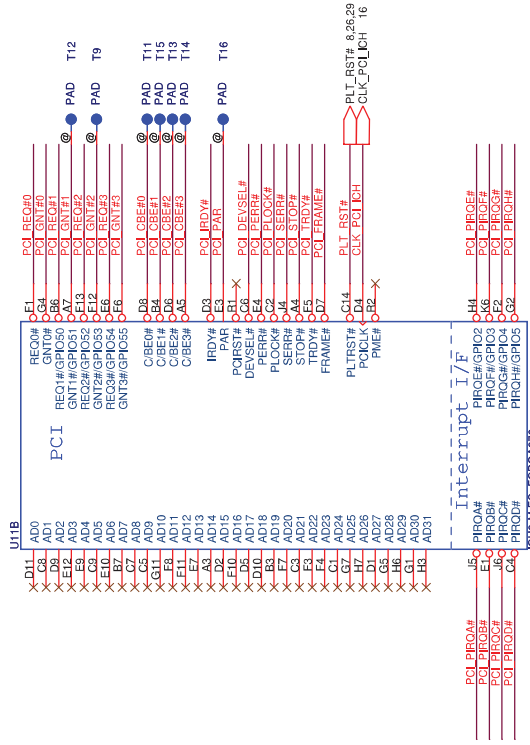
A16 Swap Override Strap		
Low= A16 swap override Enable		
High= Default*		
PCL_GNT#3		



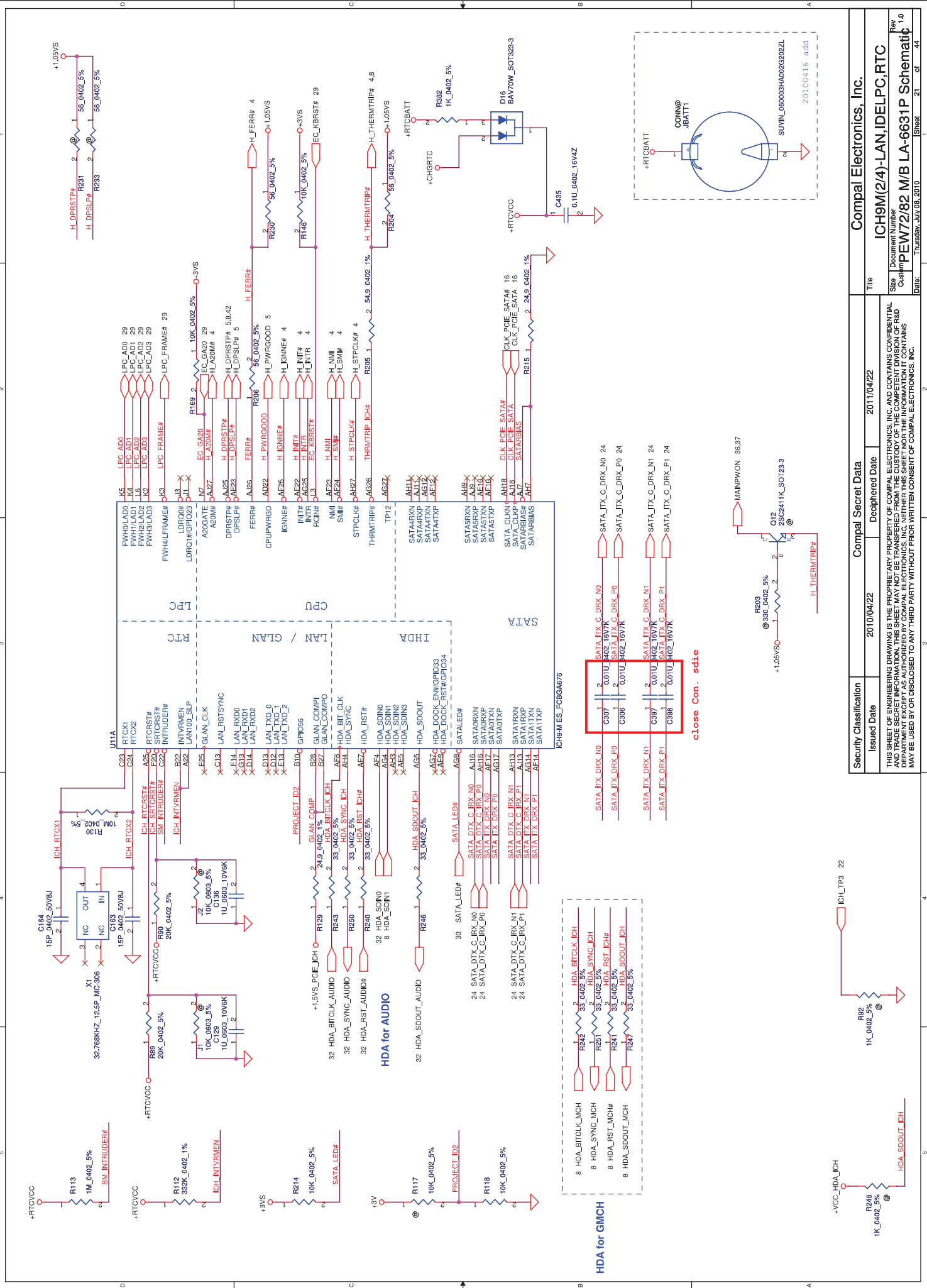
Boot BIOS Strap		
PCL_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

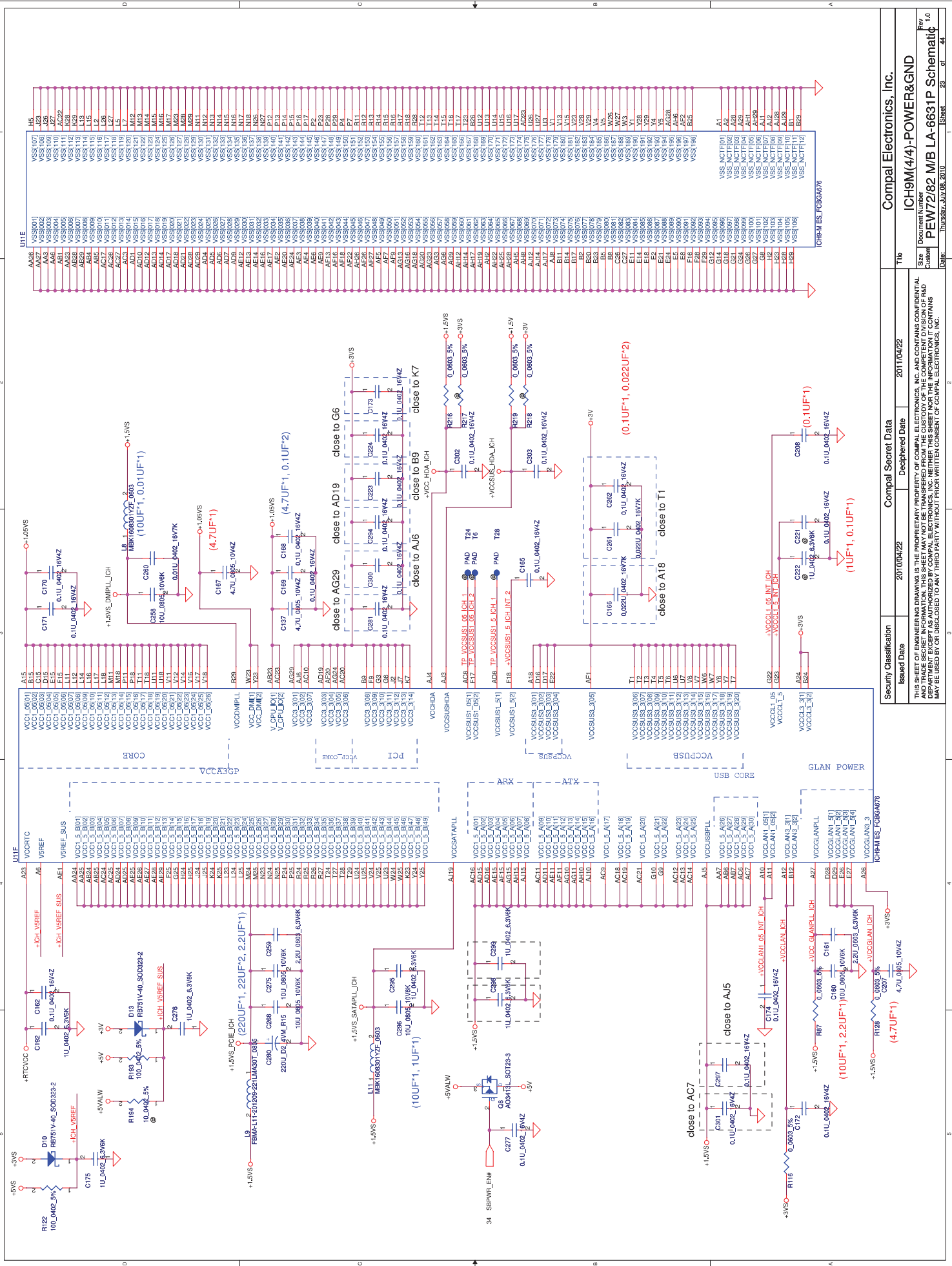


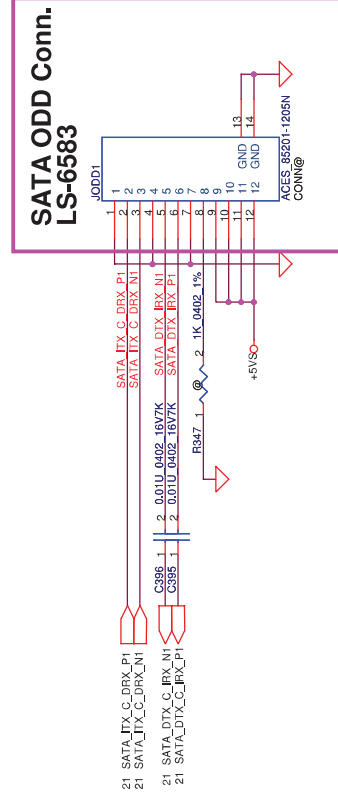
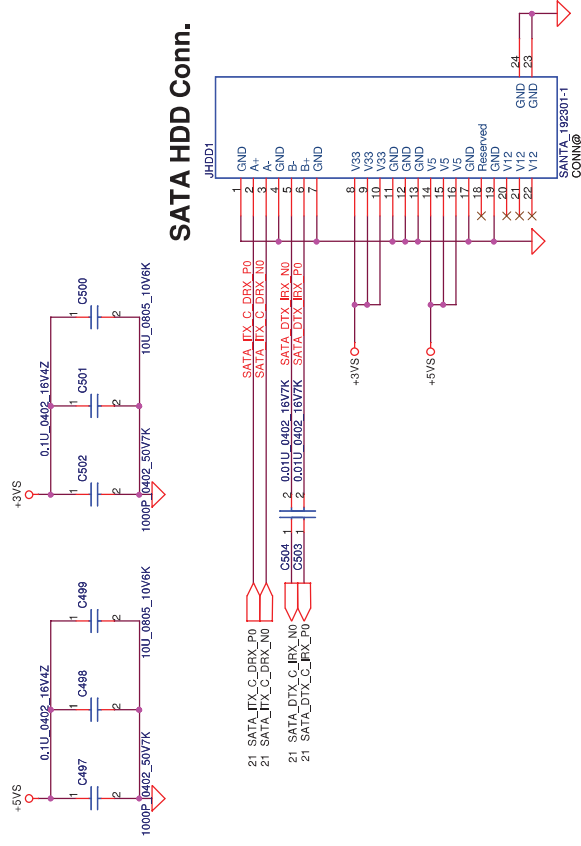
DMI for ESI-compatible operation		
Low= DMI for ESI-compatible operation		
High= Default* (Internal pull-up)		
PCL_GNT#1		



Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		2011/04/22	
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Document Number		ICH9M(1/4)-PCI			
Size		Rev			
PEW72/82 M/B LA-6631P Schematic		1.0			
DATE:		Thursday, July 08, 2010			
		Sheet 20 of 44			

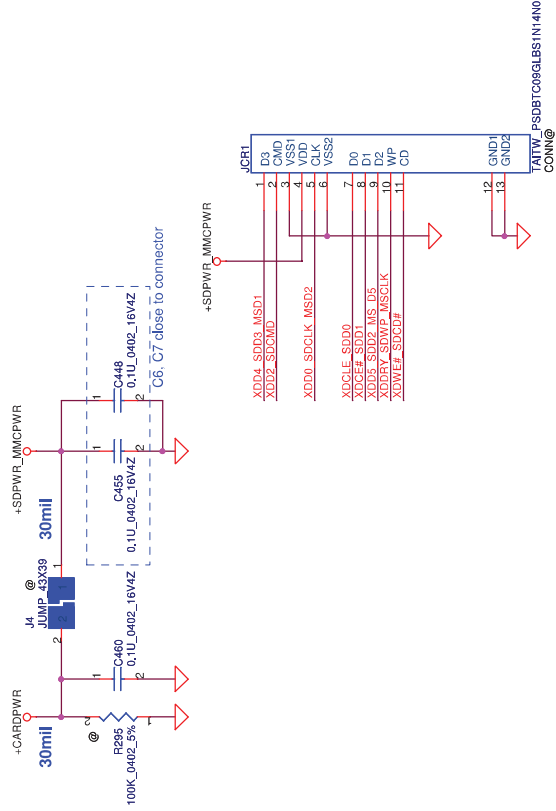




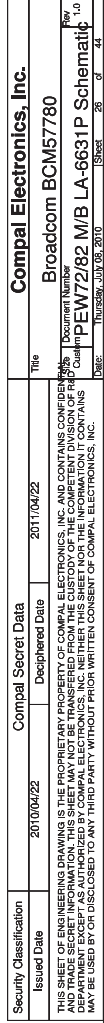


Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.
Issued Date	2010/04/22	Deciphered Date	2011/04/22	HDD & ODD Connector
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Size	Document Number	Rev		
Column	PEW72182	M/B LA-6631P	Schematic	
Date:	Thursday, July 08, 2010	Sheet	24	of 44

Card Reader Connector



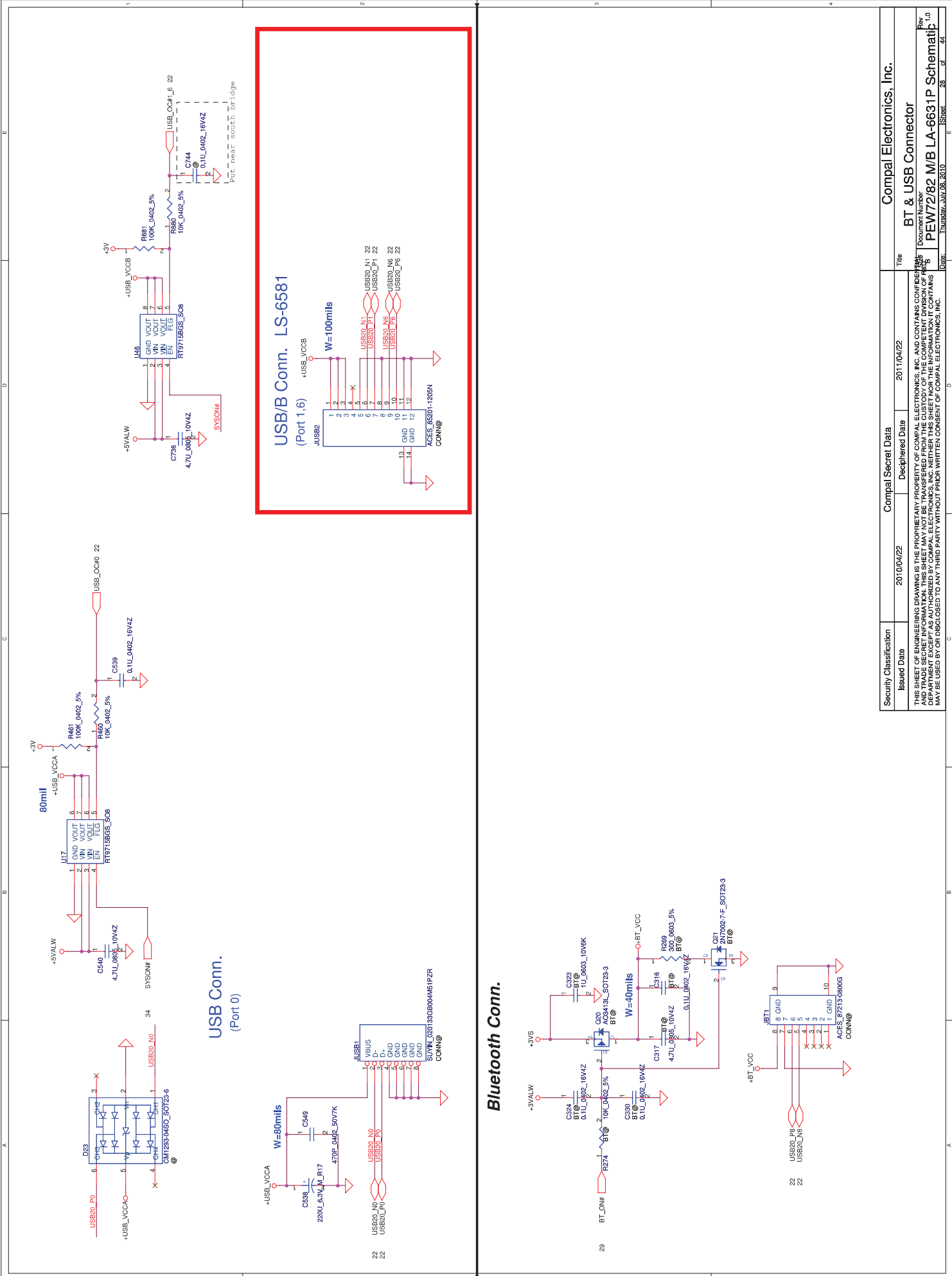
Security Classification		Compal Secret Data		Title	
Issued Date	2010/04/22	Deciphered Date	2011/04/22	CardReader RTS5137	
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</p>					
Size	Document Number	Revision			
CU000001	PEW72/82 M/B LA-6631P	Schematic 1.0			
Date:	Thursday, July 08, 2010	15	25	of	44
Sheet		Sheet			



Mini Card Power Rating				
Power	Primary Power (mA)		Auxiliary Power (mA)	
	Peak	Normal	Normal	
+3VS	1000	750		
+3V	330	250	250 (wake enable)	
+1.5VS	500	375	5 (Not wake enable)	

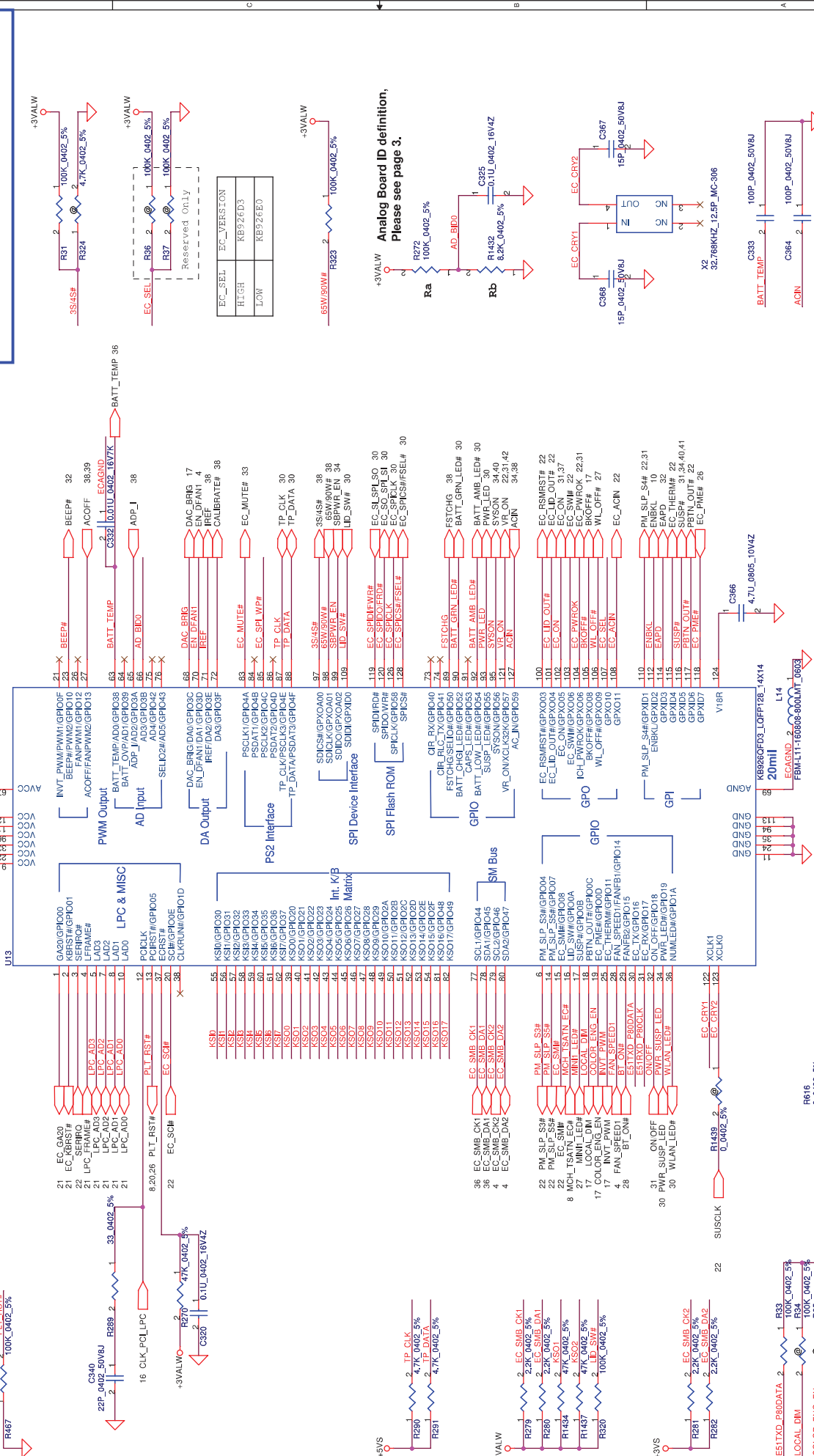
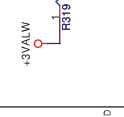
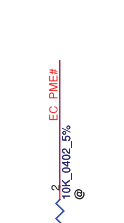
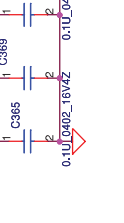
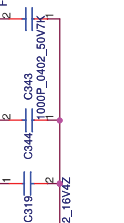
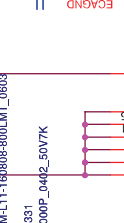
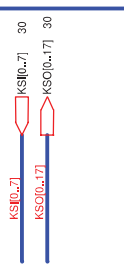
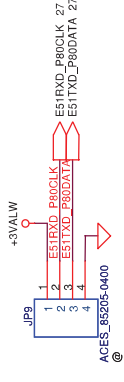


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Issued Date	2010/04/22	Deciphered Date	2011/04/22
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MINI CARD (WLAN & TV-Tuner)		Title	
Document Number	PEW7282 M/B LA-6631P Schematic	Rev	1.0
Date	Thursday, July 08, 2010	Sheet	27 of 44



For EC Tools

Place under MiniCard or DIMM



Security Classification		Compal Secret Data		Title	
Issued Date	2010/04/22	Deciphered Date	2011/04/22	EC ENE KB926	
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Size	Document Number		Rev		
B	PEW72/82 M/B LA-6631P		Schematic		
Date:	Thursday, July 08, 2010		Sheet	29	of 44

30

100K_0402_5%

EC SP1 WP#

1 @ 2

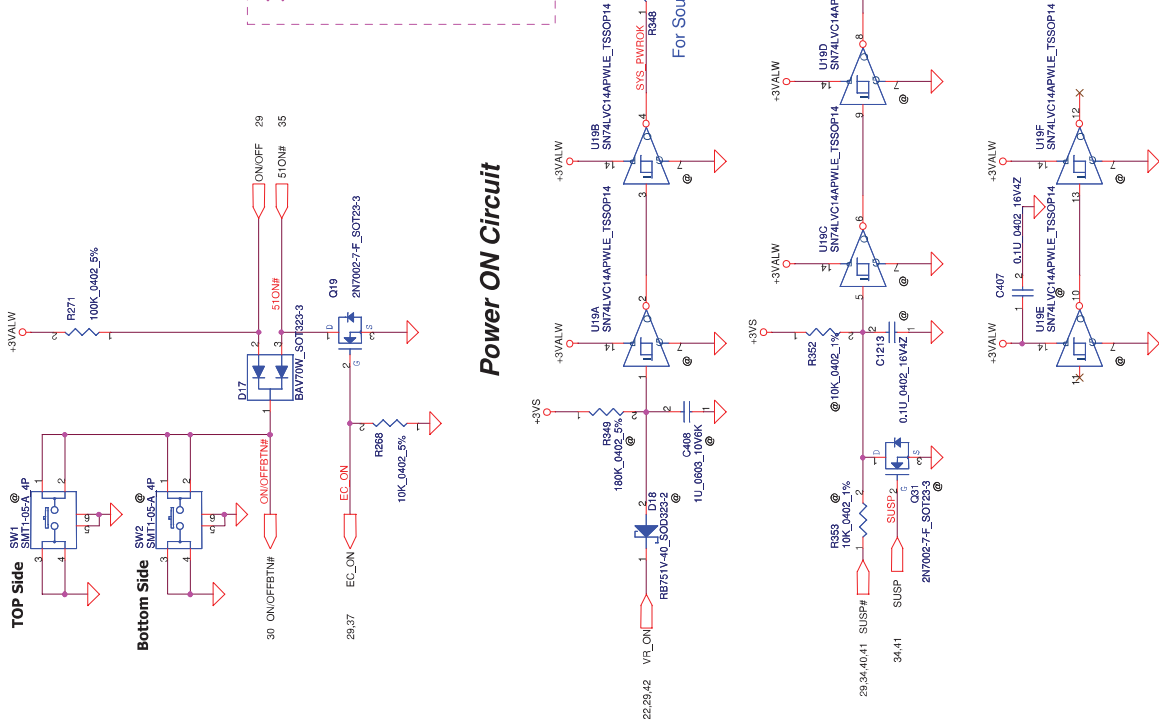
2

1 R38

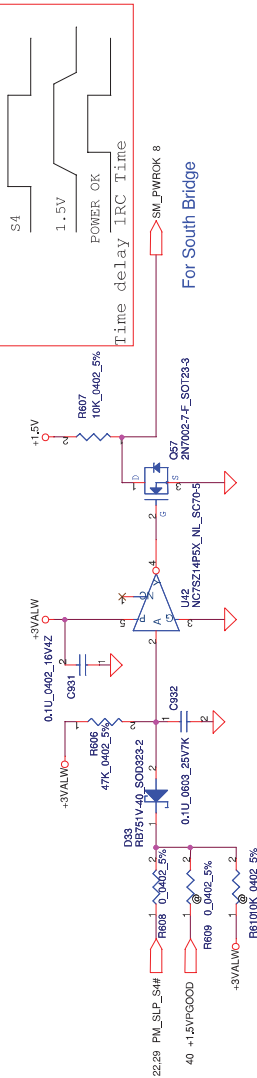
100K_0402_5%

Power Button

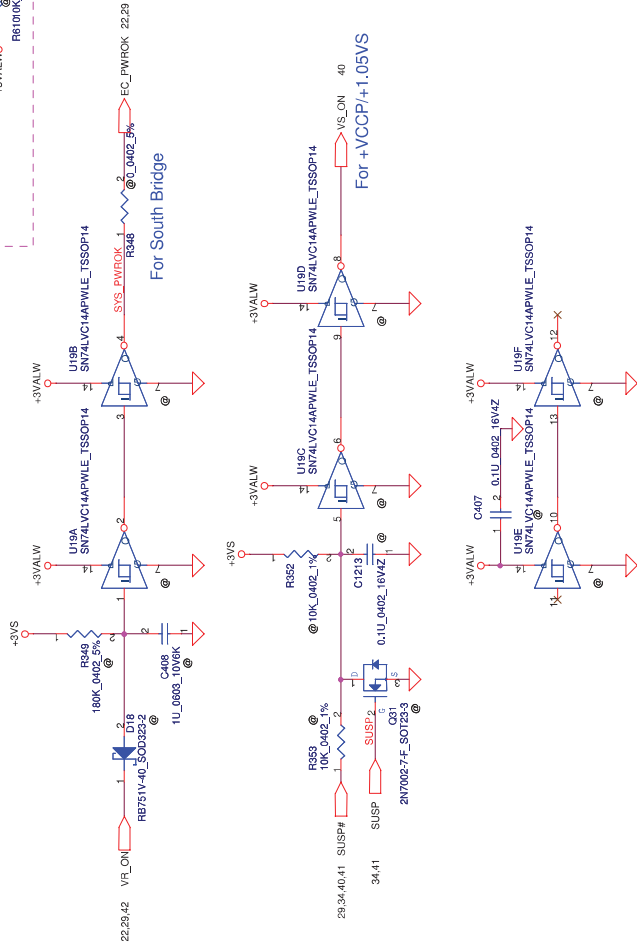
ON/OFF switch



DDR3

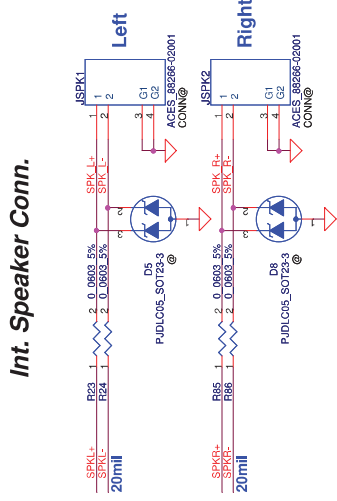


Power ON Circuit

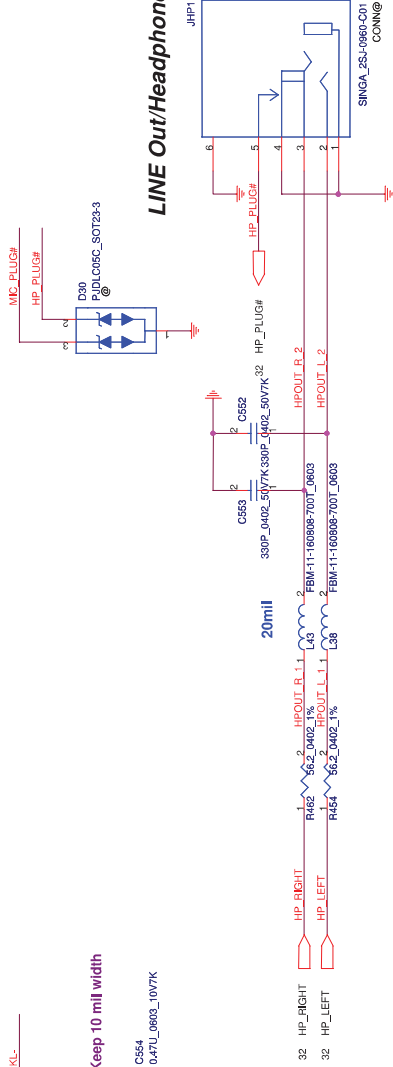


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2010/04/22	2011/04/22	2011/04/22	Compal Electronics, Inc.
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Power OK, Reset	Document Number	PEW72/82 M/B LA-6631P Schematic	Rev 1.0
2010/04/22	2011/04/22	2011/04/22	2011/04/22

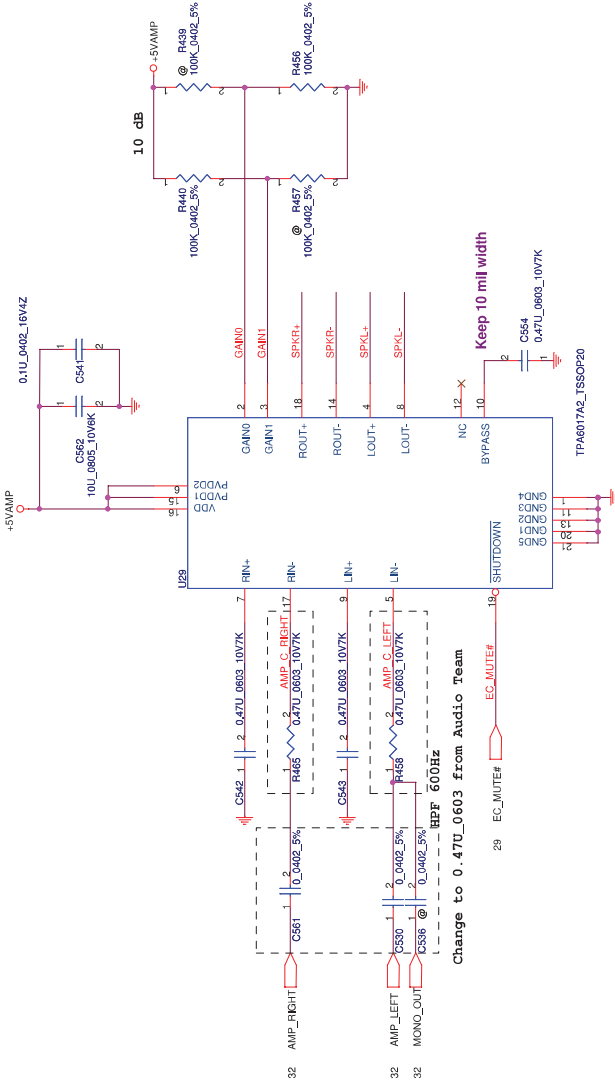
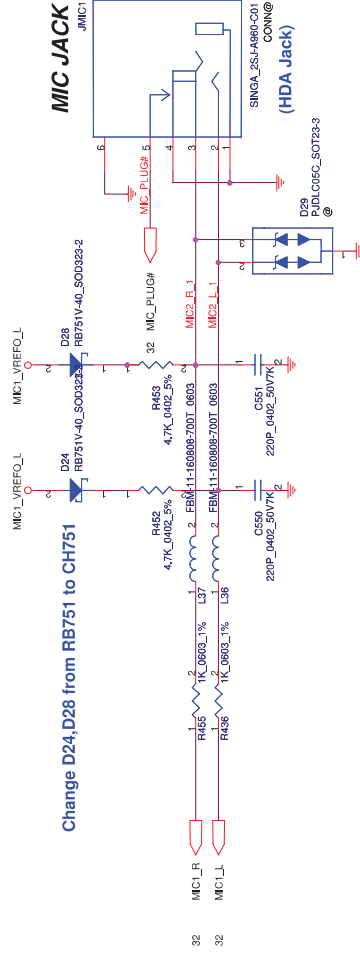
Int. Speaker Conn.



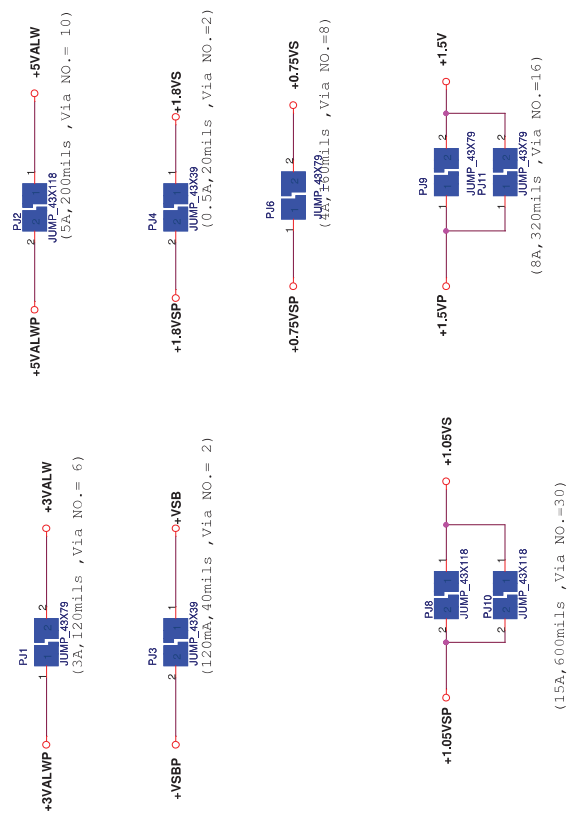
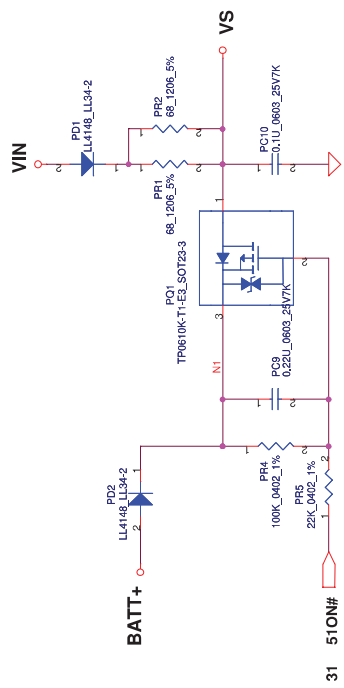
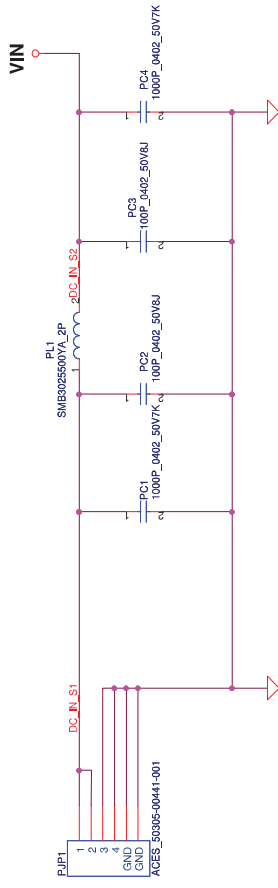
LINE Out/Headphone Out



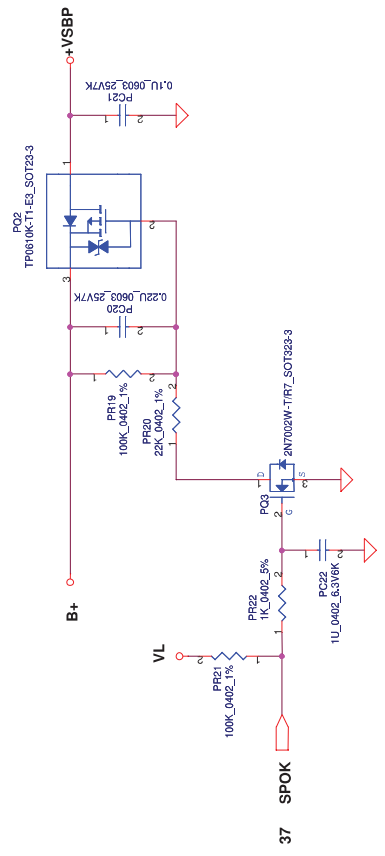
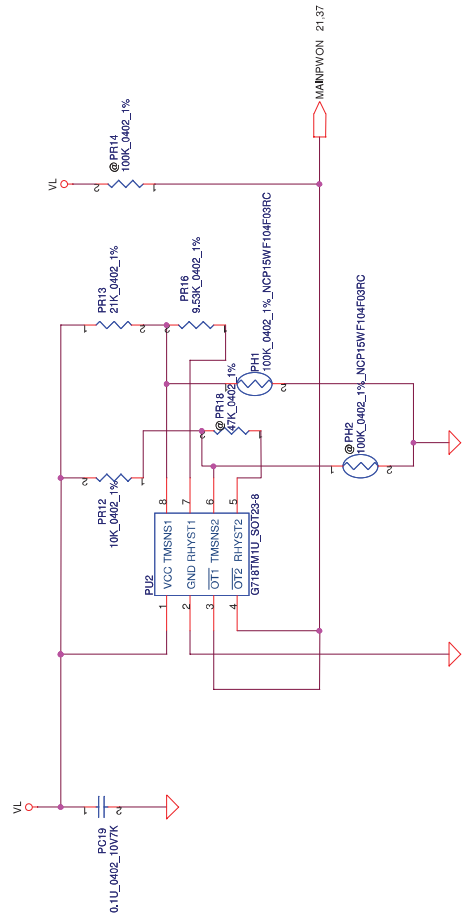
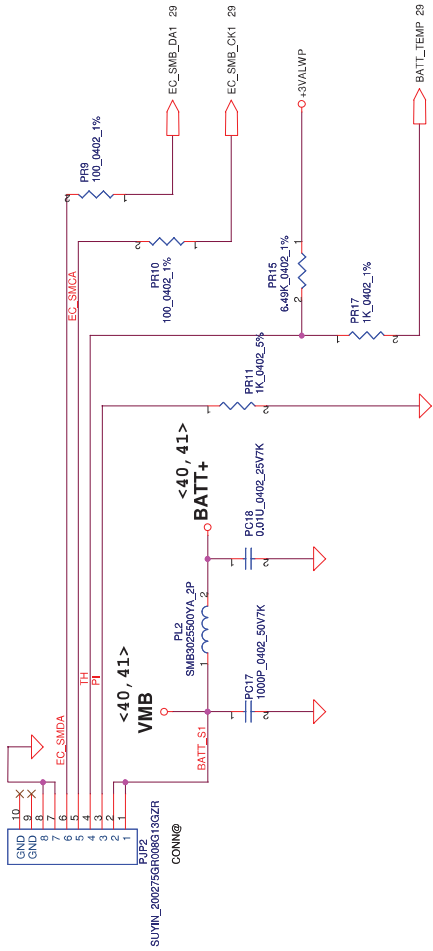
Change D24,D28 from RB751 to CH751



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Document Number				PEW72/82 M/B LA-6631P Schematic	
Rev				1	
Date				15/06/2010	

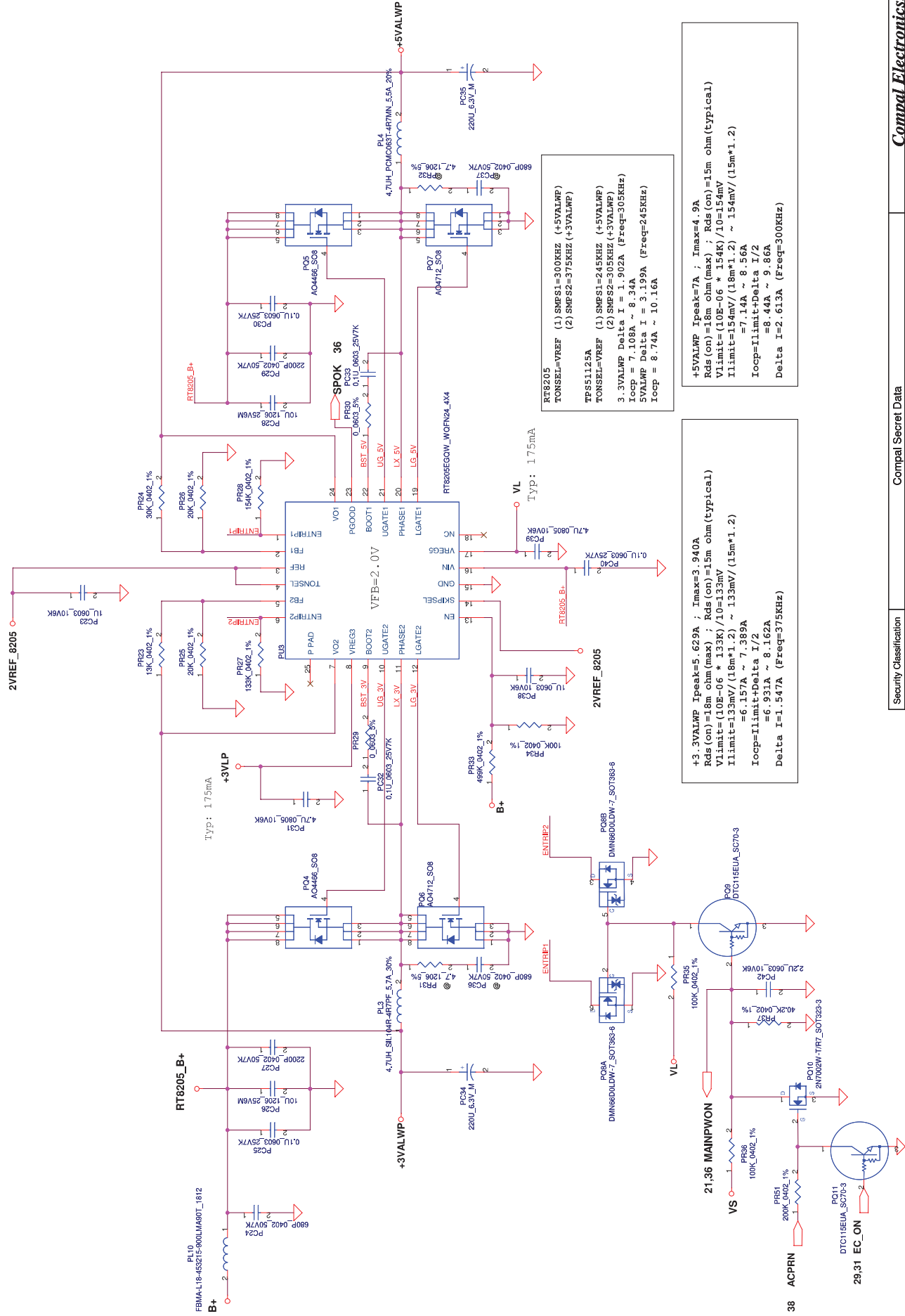


Security Classification		Compal Secret Data		Title	
Issued Date	2010/04/22	Deciphered Date	2011/04/22	Compal Electronics, Inc.	
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Issued Date	2010/04/22	Deciphered Date	2011/04/22
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BATTERY CONN / OTP			Rev
PEW72			1.0
Date: Thursday, July 03, 2010			Sheet 38 of 44

Note:
Use IFS51125 IC can remove RTC reference ID0
Use IFS51427 IC must keep RTC reference ID0



Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		2011/04/22	
2010/04/22		2011/04/22		3VALW/5VALW	
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		Custom		PEW72	
		Date		Thursday, July 08 2010	
		Sheet		37 of 44	

Compal Electronics, Inc.

3VALW/5VALW

Document Number

PEW72

Thursday, July 08 2010

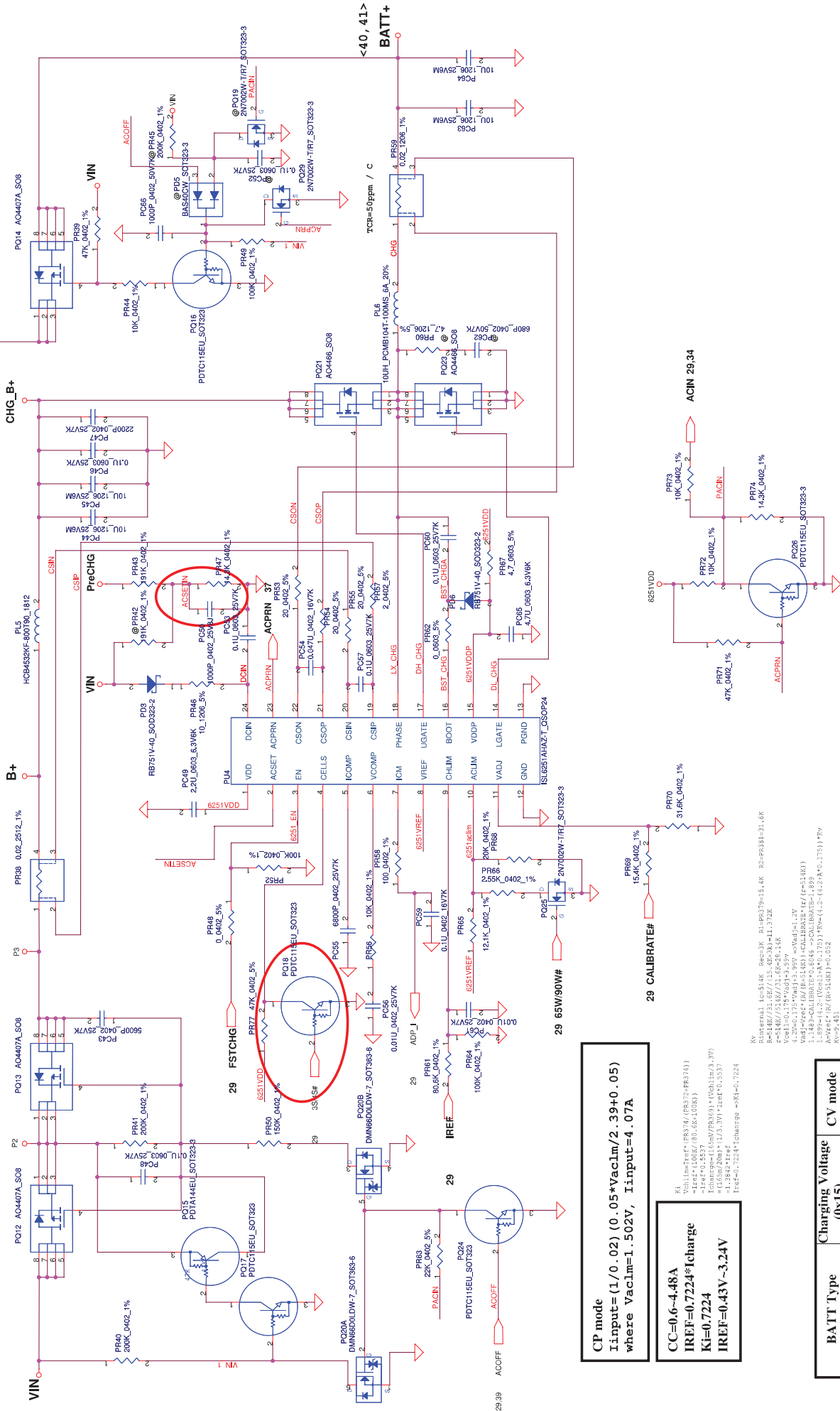
Rev

1.0

I_{ada}=0-4.74A (90W/19V=4.736A)
I_{ada}=0-3.42A (90W/19V=3.421A)

ADP_I = 19.9*I_{adap}*R_{sense}

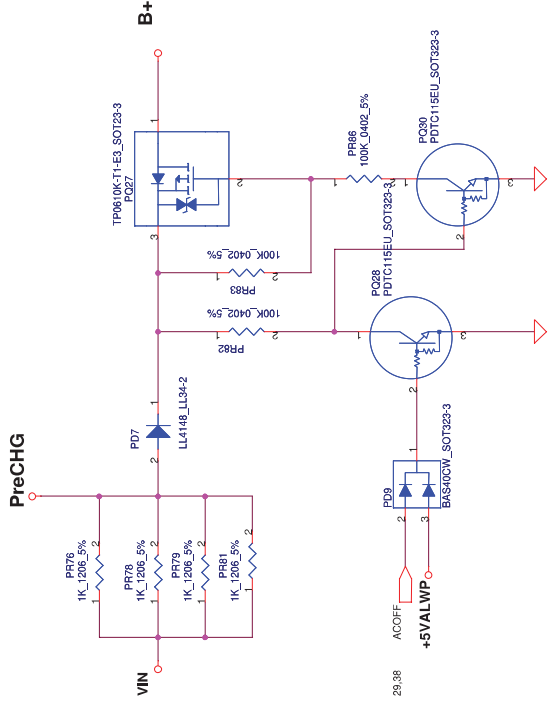
CP = 85%*I_{ada} ; CP = 4.07A
CP = 85%*I_{ada} ; CP = 2.91A



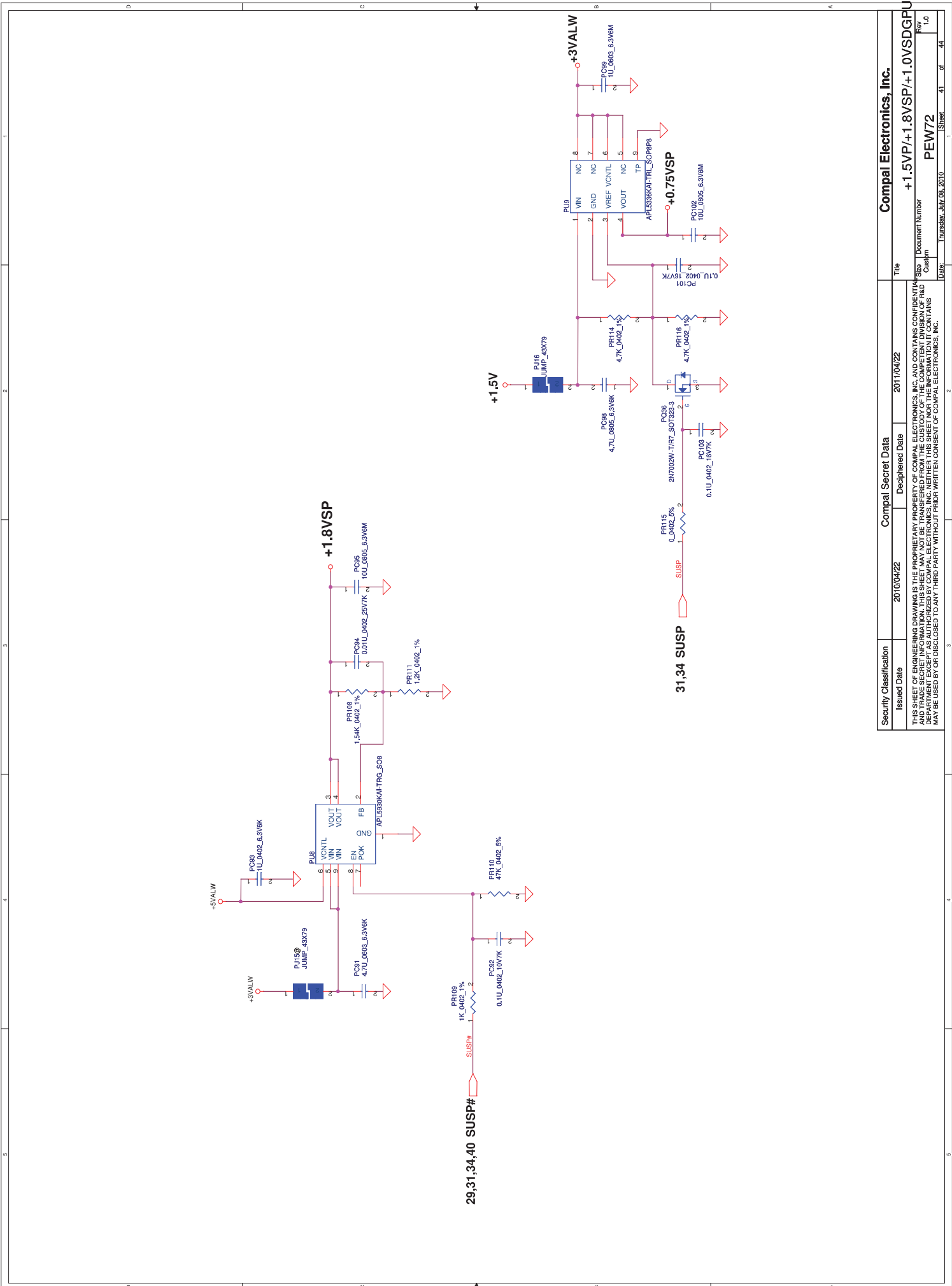
CP mode
Input=1/0.02 (0.05*VacIm/2.39+0.05)
where VacIm=1.502V, Iinput=4.07A

CC=0.6-4.48A
IREF=0.7224*I_{charge}
KI=0.7224
IREF=0.43V-3.24V

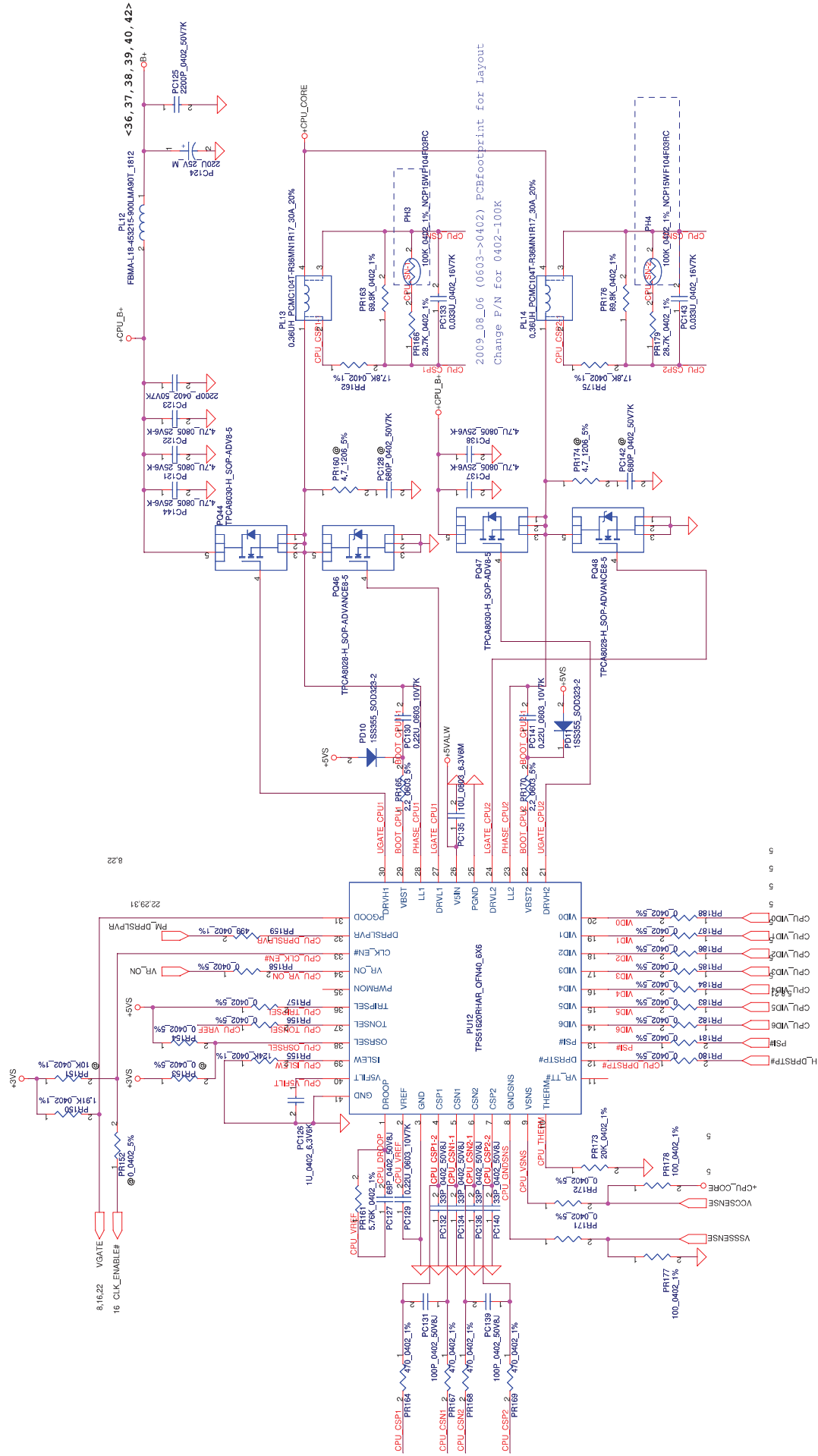
BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S Li-ON Cells	12600mV	12.60V



Security Classification		Compal Secret Data		Title	
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	Size	Custodian			
	Rev	1.0			
Date: Thursday, July 08, 2010					Sheet 38 of 44



Security Classification		Compal Secret Data		Title	
Issued Date	2010/04/22	Deciphered Date	2011/04/22	Compal Electronics, Inc.	
+1.5VP/+1.8VSP/+1.0VSDGPU					
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				Size	Document Number
				1.0	PEW72
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				Sheet	41 of 44



Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		+CPU CORE	
2010/04/22		2011/04/22		PEW72	
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		1.0		Custodian	
		Thursday, July 08, 2010		Sheet 42 of 44	

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	add 3S/4S pin function	add 4 cell battery	0.2	45	add PQ18 PDTC115PU_SOT323 (SB301150200) and PR77 47K +-5% 0402 (SD028470284)	2010/06/11	EVT
2	ACSETIN net	ACSETIN net no connect	0.2	45		2010/06/11	EVT
3	1.5V enable	1.5V enable BOM error	0.2	45	add PR32 and delete PR90 0_0402_5% (SD028000080)	2010/06/11	EVT
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
16							
17							

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/04/22	Deciphered Date	2011/04/22	PIR (PWR)	
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				Custodian	PEW72/82 M/B LA-6631P Schematic
				Date	Thursday, July 08, 2010
				Sheet	43 of 44

A --> C Change List

- 20100622-----
1. Change U48 to SA00002KI00 (EON EN25F16-100HIP)
2. Populate D11, D12
3. Populate R132, C194, R136, C225, R354, C416
20100618-----
1. Page 30, For EMI require populate C31, C32, C33, C34, C28, C35, C36, C27, C30, C29, C39, C40, C41, C42, C43, C24, C46, C47, C48 C23, C22, C21
2. Page 12, Populate C483
20100617-----
1. Add T19, T25 for boundary scan (CIT Factory)
2. Page 34, Add 0.1U_0402_16V4Z x 16 for +3VS/+5VS/+R_CRT_VCC/+HDMI_5V_OUT
C548, C555, C563, C564, C565, C566, C567, C568, C569, C570, C571, C572, C573, C574, C575, C576, C577
3. Page 29, Reserved R38, R616 for SPI_WP#
20100615-----
1. Page22, Add C745 for USB_OC#1_6 at chipset side.
2. Page28, Change C744 BOM Structure to @
20100614-----
1. Page29, Change U13 to KB926QFD3 (SA00001J580)
Change R1432 to 8.2K_0402_5% (SD028820180)
2. Page16, Change U16 to ICS9LPRS387 (SA000020H10)
Change BOM Structure of L33 and R401 to @
Populate L32 and R400
3. Page31, Change BOM Structure of SW1 and SW2 to @
4. Change U7, U8, U43 to MC74VHC1G08DFT2G (SA000000H00)
5. Update Power Schematics

C --> MP Change List

- 20100709-----
1. Page33, Change C561, C530, C536 to 0 ohm (SD028000080)
Change R465, R458 to 0.47U_0603 (SE080474K80)
20100708-----
1. Page28, Unpopulate D23 (follow ESD suggestion)
20100706-----
1. Page29, Populate R289 and C340.
2. Page30, Unpopulate C21 ~ C43 and C46 ~ C48.

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